CMOS Transistor

Stick diagrams:

Stick diagrams are used to convey layer information through the use of a colour code for example in NMOS design.

- Green for n- diffusion
- Red for poly silicon
- Blue for metal
- Yellow for implant
- Black for contact areas
- The designer can draw a layout using coloured lines to represent the various process layers such as diffusion, metal and poly silicon.
- Where poly silicon crosses the diffusion, transistors are created and where metal wires join diffusion or poly silicon, contacts are formed.
- A stick diagram is a cartoon of a chip layout. They are not the exact models of layout.

- The stick diagram represents the rectangles with lines which represents wires are component symbols.
- The colour cooling has been complemented by monochrome encoding of the lies so the black and white copies of stick diagrams do not lose the layer information.
- The colour and monochrome encoding scheme used has been evolved to cover NMOS and CMOS processes.
- To illustrate the stick diagram inverter circuits are presented below in NMOS, and in P well CMOS technology.

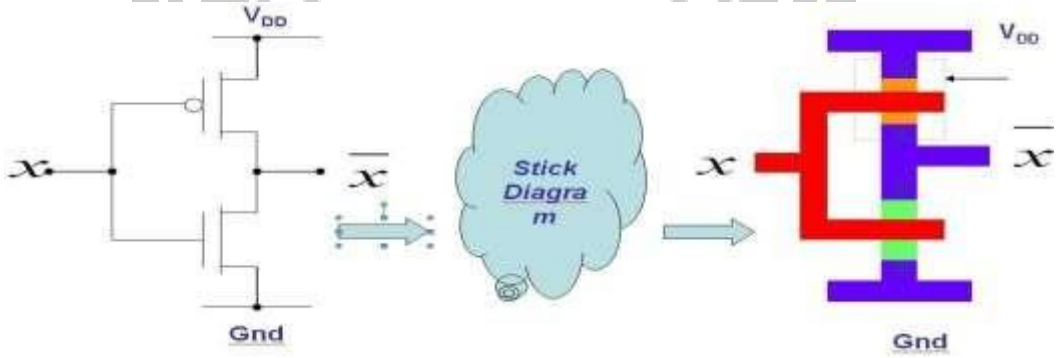

Figure 1.2.1 : Stick diagrams

[Source: Wayne Wolf, ―Modern VLSI Design: System On Chip ….]

- Having conveyed layer information and topology by using stick or symbolic diagrams. These diagrams relatively easily turned into mask layouts.
- The below diagram stressing the ready translation into mask layout form. In order that the mask layout produced during design will be compactible with the fabrication process.

  Aser of design rules are set out for layouts.

Stick diagram using NMOS Deisgn:

We consider single metal, single poly silica NMOS technology. The layout of NMOS involves.

- N-diffusion and other thin oxide regions- green
- Polysilicon - red
- Metal -blue
- Impant -yellow
- Contacts - black or brown

A transistor is formed wherever poly silicon crosses n-diffusion and all diffusion wires are n-type. The various steps involved in the design style are.

Step1: Draw the metal VDD and GND rails in parallel allowing enough space between them for the other circuit element which will be required.

Step 2: Draw the thinox paths between the rails for inverters and inverter based logic.

Step 3: Draw the pull up structure which comprises a depletion mode transistor interconnected between the output point and VDD.

Step 4:Draw the pull down structure comprising an enhancement mode structure interconnected between the output point and GNO.

Step 5: Signal paths may be switched by pass transistor, and along signal paths often require metal buses.

Design Rules and layout:

The design rules primarily address two issue

1) The geometrical reproduction of features that can be reproduced by the mask-making and lithographical process.
2) The interactions between different layers. There are several approaches that can be taken in describing the design rules. These include

- Micron design rules:
- Stated at some micron resolution
- Usually given as a list of minimum feature sizes and spacings for all masks required in a given process.
- Normal style for industry.

- Lambda (λ) based design rules

- These rules popularized by Mead and Conway are based on a single parameter, λ which charactized the linear feature- the resolution of the complete wafer implementation process – and permits first order scaling.
- They have been widely used, particularly in the educational context and in the design of multi project chips.

Layout (λ) based design Rules:

The lambda, λ design rules are bases on mead and Conway work and in general, design rules and layout methodology are based on the concept of λ which provides a process and feature size. Independent way of making mask dimensions to scale.

- All paths in all layers will be dimensioned in λ units and sub-sequently λ can be allocated an appropriate value compactible with the feature size of the fabricalion process.
- Design rules can be conveniently set out in diagrammatic form as shown below.

Contact cuts:

The contacts between layers are set out as shown below. Here it will be obserred that connection can be made between two or, in the case of NMOs design, three layers.

1) Metal to poly silicon or to diffusion

There are three possible approaches for making contacts between poly silicon and diffusion in NMOS circuits. There are

i) Poly silicon to metal then metal to diffusion

ii) Buried contact poly silicon to diffusion

iii) Butting contact.

- The 2 λ x2 λ contac cut indicates and area in which the oxide is to be removed down to the underlying polysilicon or diffusion surface.
- When the deposition of the metal layer takes place, the metal is deposited through the contact cut areas on to the underlying areas so that contact is made between

the layers.

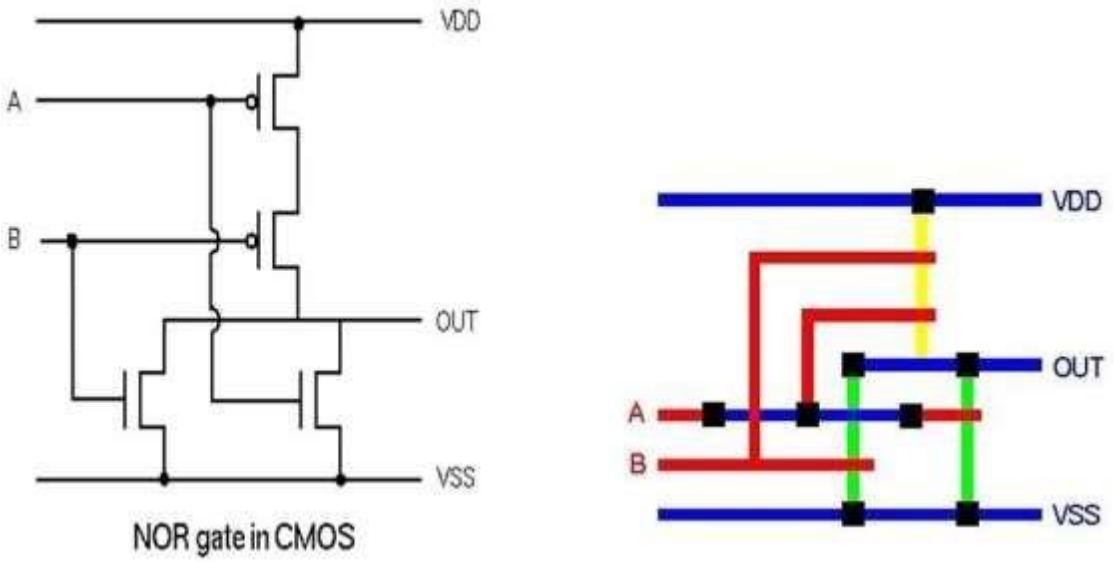

Figure 1.2.2: Stick diagrams

[Source: . Neil H.E. Weste, David Money Harris —CMOS VLSI Design ….]