4.9 Carbon Nano Tube Field Effect Transistor (CNTFETs)

Carbon nanotube field effect transistor (CNTFETs) uses semi conducting carbon nanotube as the channel. Both p-channel and n-channel devices can be made from nanotubes. The physical structure of CNTFETs is very similar to that of MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics.

The carbon nanotube is one-dimensional, which greatly reduces the scattering probability. As a result, the device may operate in ballistic regime.

The nanotube conducts essentially on its surface where all the chemical bonds are saturated and stable. In other words, there are no dangling bonds which form interface states. Therefore, there is no need for careful passivation of the interface between the nanotube channel and the gate dielectric, i.e. there is no equivalent of the silicon/silicon dioxide interface.

The Schottkey barrier at the metal-nanotube contact is the active switching element in an intrinsic nanotube device. With these unique features CNTFET becomes a device of special interest.

Type of CNTFET

The field effect transistors made of carbon nanotubes so far can be classified into:

a) Back gate CNTFET
b) Top gate CNTFET
c) Wrap-around gate CNTFETs
d) Suspended CNTFETs

a) Back-gated CNTFET's

The earliest techniques for fabricating carbon nanotube (CNT) field-effect transistors involved pre-patterning parallel strips of metal across a silicon dioxide substrate, and then depositing the CNTs on top in a random pattern.

The semiconducting CNTs that happened to fall across two metal strips meet all the requirements necessary for a rudimentary field-effect transistor. One metal strip is the "source" contact while the other is the "drain" contact. The silicon oxide substrate

can be used as the gate oxide and adding a metal contact on the back makes the semiconducting CNT gateable.

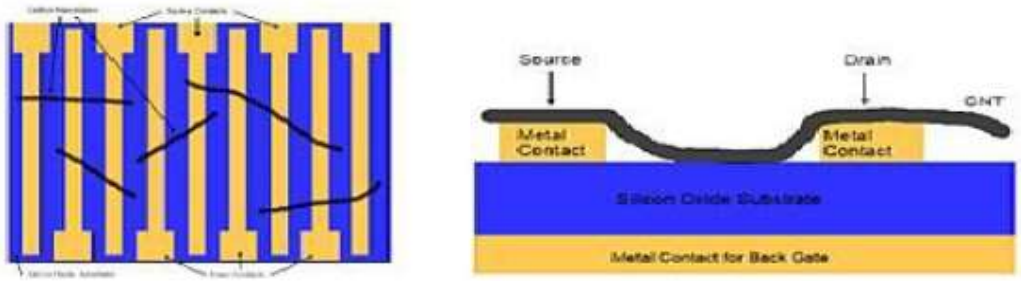

Fig 4.9.1 Top and side view of carbon nanotubes deposited on a silicon oxide substrate pre-patterned with source and drain contacts.

(source : https://core.ac.uk/download/pdf/61802786.pdf)

The types of back gate CNTFETs discussed so far have high contact resistances (≥1 MΩ), which led to a low trans conductance gm (=dI/dVG) of about 10 - 9A/V. This large contact resistance results from the weak van der Waals coupling of the devices to the noble metal electrodes in the 'side-bonding' configuration used. Here the SWNT is dispersed on top of the SiO2 film, and then source and drain electrodes made of transition metals compatible with silicon technology, such as Ti or Co, are fabricated on SWNT. Subsequent anneals at 400º C (Co) and, or at 820º C (Ti) in an inert ambient, form low resistance Co contacts or TiC contacts at the source and drain electrodes.

b) Top-gated CNTFET's

In the first step, single-walled carbon nanotubes are solution deposited onto a silicon oxide substrate. Individual nanotubes are then located via atomic force microscope or scanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high resolution electron beam lithography. A high temperature anneal step reduces the contact resistance by improving adhesion between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric, completing the process. Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case. Also, due to the thinness of the gate dielectric, a larger electric field can be generated

with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally preferred over back-gated CNTFETs, despite their more complex fabrication process.

c) Wrap-around gate CNTFET's

Wrap-around gate CNTFETs, also known as gate-all-around CNTFETs In this device, instead of gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated. This should ideally improve the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

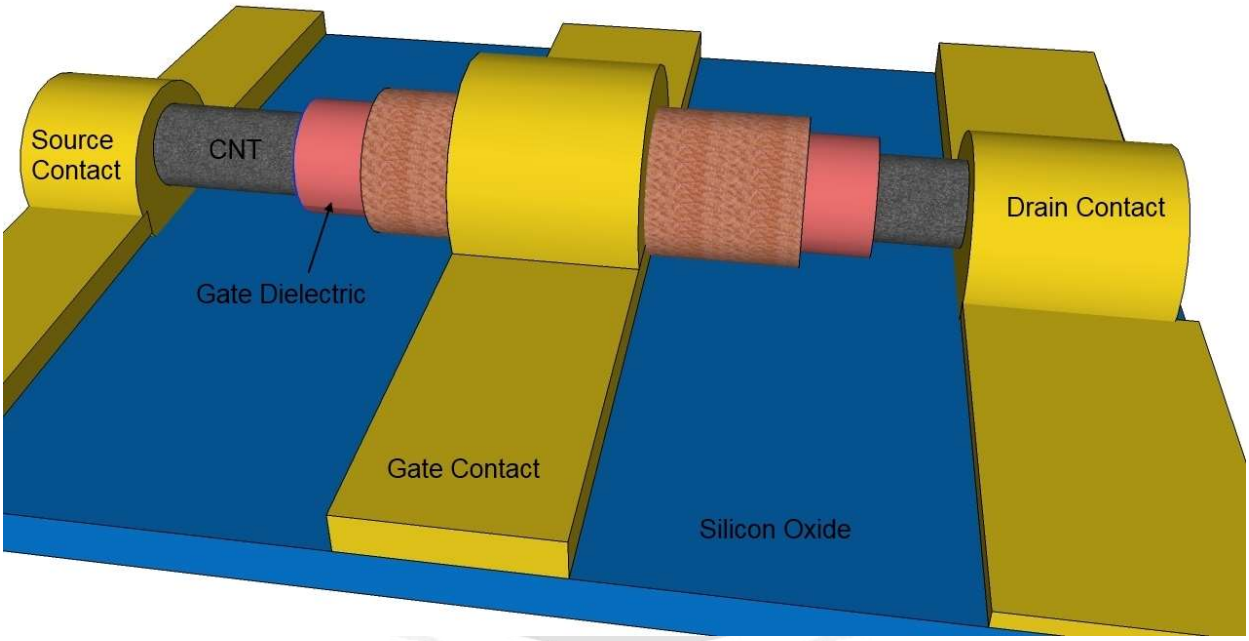

Fig 4.9.2 Wrap-around gate CNTFET

(source : https://core.ac.uk/download/pdf/61802786.pdf)

Device fabrication begins by first wrapping CNTs in a gate dielectric and gate contact via atomic layer deposition. These wrapped nanotubes are then solution-deposited on an insulating substrate, where the wrappings are partially etched off, exposing the ends of the nanotube. The source, drain, and gate contacts are then deposited onto the CNT ends and the metallic outer gate wrapping.

d) Suspended CNTFET's

CNTFET device geometry involves suspending the nanotube over a trench to reduce contact with the substrate and gate oxide. This technique has the advantage of reduced scattering at the CNT-substrate interface, improving device. There are many

methods used to fabricate suspended CNTFETs, ranging from growing them over trenches using catalyst particles, transferring them onto a substrate and then under-etching the dielectric beneath , and transfer-printing onto a trenched substrate.

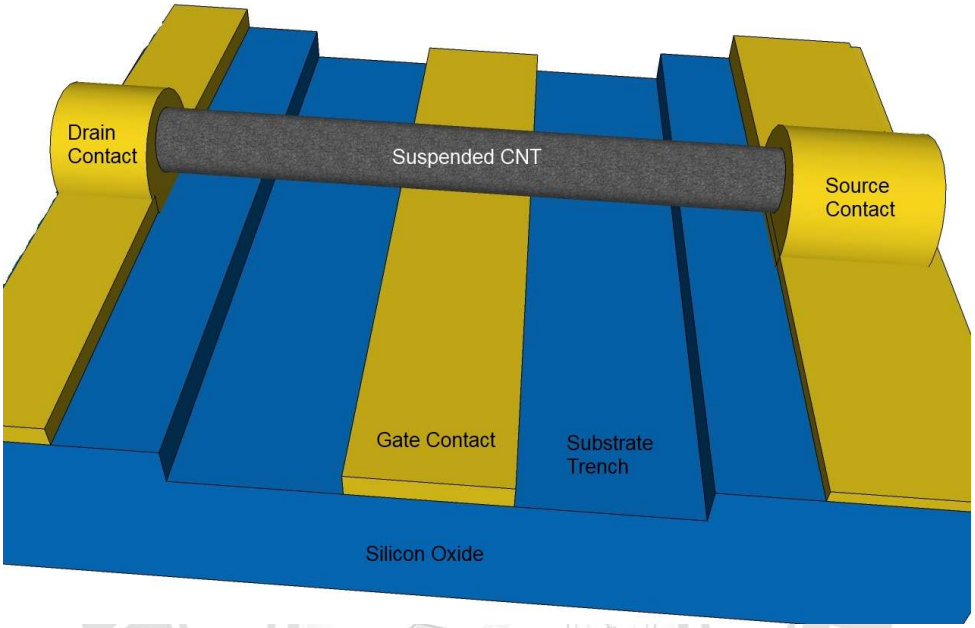

Fig 4.9.3 Suspended CNTFET device.

(source : https://core.ac.uk/download/pdf/61802786.pdf)

The main problem suffered by suspended CNTFETs is that they have very limited material options for use as a gate dielectric (generally air or vacuum), and applying a gate bias has the effect of pulling the nanotube closer to the gate, which places an upper limit on how much the nanotube can be gated. This technique will also only work for shorter nanotubes, as longer tubes will flex in the middle and droop towards the gate, possibly making touching the metal contact and shorting the device. In general, suspended CNTFETs are not practical for commercial applications, but they can be useful for studying the intrinsic properties of clean nanotubes.

Characteristics of CNTFET's

The drain I-V characteristics in 2D are shown in fig. The saturation current at VGS = 0.5 V is around 6 μA, which is not inconsistent with values emerging from recent experimental work.

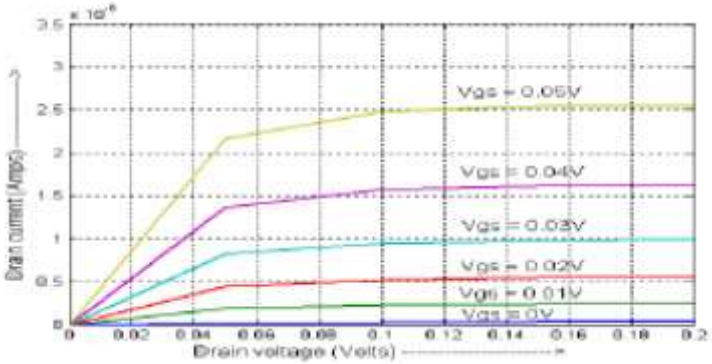

Fig 4.9.4 CNTFET sub threshold Drain characteristics.

(source : https://core.ac.uk/download/pdf/61802786.pdf)

Drain I-V characteristics exhibited dependence of saturation drain current on temperature. When CNTFET is cooled, drain saturation currents were lightly decreased.

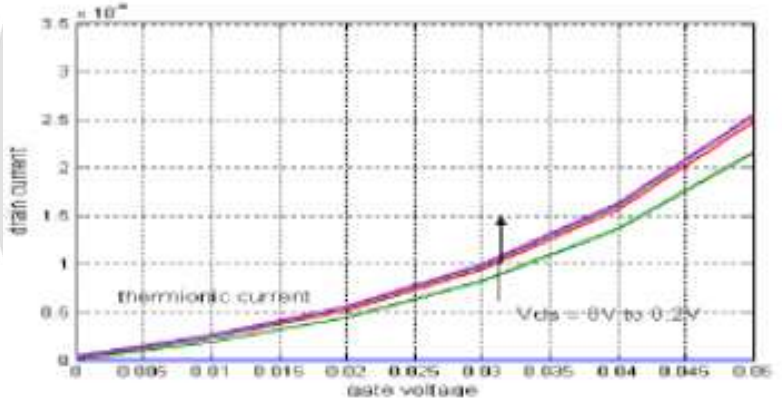

Fig 4.9.5 CNTFET sub threshold Transfer characteristics

(source : https://core.ac.uk/download/pdf/61802786.pdf)