

3.4 OPERATION OF BASIC PHASE LOCKED LOOP

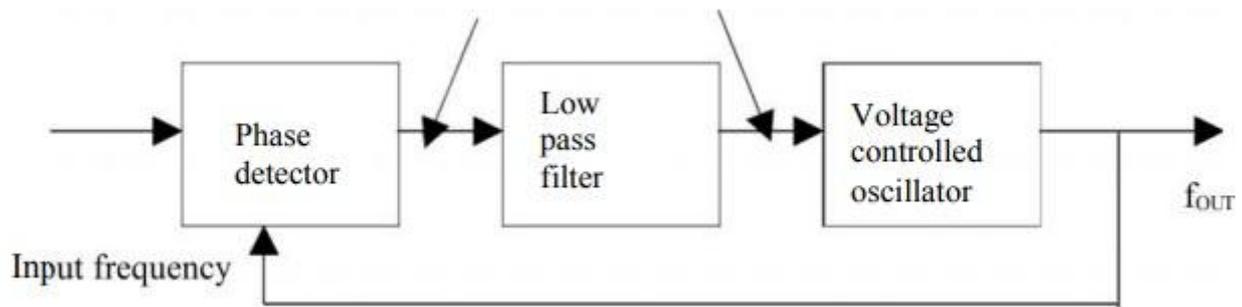


Figure 3.4.1. Block Diagram of PLL

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The PLL consists of i) Phase detector ii) LPF iii) VCO. Figure 3.4.1 shown above is the block diagram of PLL. The phase detector or comparator compares the input frequency f_{IN} with feedback frequency f_{OUT} . The output of the phase detector is proportional to the phase difference between f_{IN} & f_{OUT} . The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage. The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO. The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies. PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action.

If an input signal vs of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency of the incoming signal to that of the output v_o of the VCO. The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_o)$ is removed by the low pass

filter and the difference frequency component is amplified then applied as control voltage v_c to VCO.

The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o . Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ . This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0 .

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Lock-in Range: Once the PLL is locked, It can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock in range or tracking range.

CLOSED LOOP ANALYSIS OF PLL

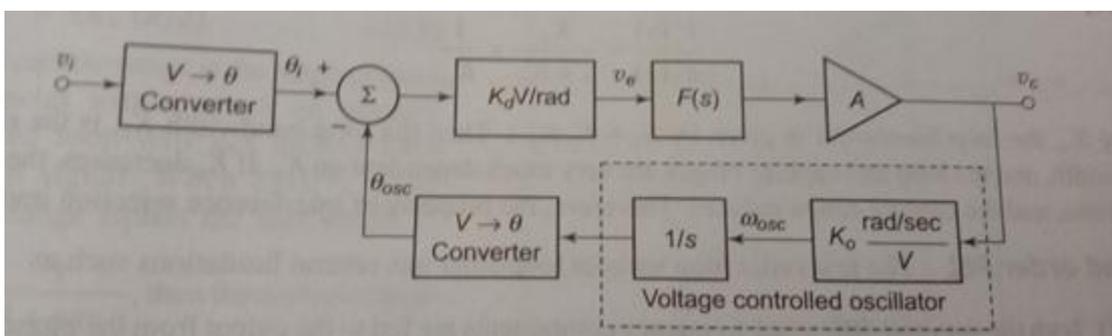


Figure 3.4.2. Detailed block diagram of PLL

[source: "Linear Integrated Circuits" by S. Salivahanan & V.S. Kanchana Bhaskaran, Page-417]

Figure 3.4.2 shown above is the detailed block diagram of PLL. The i/p sinusoidal gain V_i is given as

$$V_i = V_p \sin(\omega t + \theta)$$

If the phase shift of the signal at the VCO o/p is θ_{osc} , then the average value of the o/p of phase detector is

$$V_e = K_d(\theta_i - \theta_{osc})$$

where θ_i & $\theta_{osc} \rightarrow$ phase shift

The phase of the signal at the o/p of VCO as a function of time is equal to integral of the VCO o/p frequency & can be expressed as

$$\omega_{osc(t)} = \frac{d\theta_{osc(t)}}{dt}$$

$$d\theta_{osc(t)} = \omega_{osc(t)} dt$$

$$\int d\theta_{osc(t)} = \int \omega_{osc(t)} dt + \theta_{osc} \text{ at } t=0$$

$$\theta_{osc(t)} = \int \omega_{osc(t)} dt + \theta_{osc} \text{ at } t=0$$

The integral component is represented as $1/S$ inside the VCO block. Oscillator frequency ω_{osc} & the dc control voltage V_c are related by

$$\omega_{osc} = \omega_c + K_o V_c$$

where, $\omega_c \rightarrow$ centre or free running angular frequency,

that results when $V_c = 0$ & K_o is the VCO gain in rad/sec per volt.

Then the closed loop transfer function of PLL

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_d F(s) A}{1 + K_d A F(s) \frac{K_o}{s}} = \frac{S K_d F(s) A}{S + K_d A F(s) K_o}$$

Response of the loop to frequency variation at i/p than phase.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(s)}{S\theta_i(s)} = \frac{K_d F(s)A}{S + K_d A F(s)K_o}$$

$$\omega_i = \frac{d\theta_i}{dt} \quad \& \quad \omega_i(s) = s\theta_i(s)$$

$F(s)=0$, with the loop having a first order low pass frequency response.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_v}{S + K_v} \times \frac{1}{K_o}$$

$K_v \rightarrow$ loop bandwidth.

$$K_v = K_o K_d A$$

SECOND ORDER PLL

The first order loop without loop-filter has several limitations.

1. Both the sum & difference frequency components are fed to the o/p from the phase detector.
2. All out-of band interfering signals from the i/p will appear shifted in frequency at the o/p.

The most common configuration of monolithic PLL in the second order loop with a loop-filter $F(s)$ of a simple single-pole LPF realized with a resistor R & a Capacitor C in Figure 3.4.3.

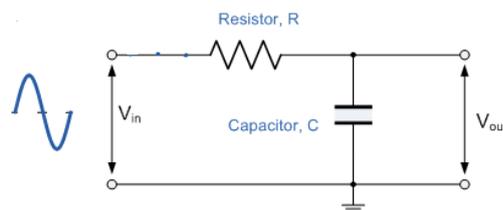


Figure 3.4.3 Single pole loop filter

[source: https://www.electronics-tutorials.ws/filter/filter_2.html]

$$F(s) = \frac{1/SC}{R + 1/SC} = \frac{1}{1 + SRC}$$

$$= \frac{1}{1 + S/\omega} = \frac{1}{1 + S\tau}$$

$$\omega = \frac{1}{RC} = \frac{1}{\tau}$$

The resulting block diagram of the second order PLL using single-pole loop filter is shown in Figure 3.4.4.

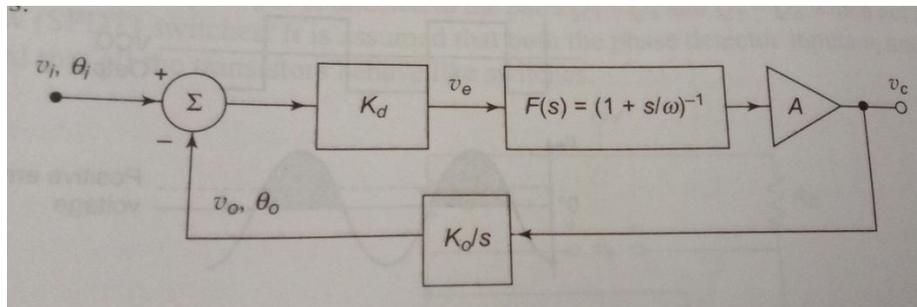


Figure 3.4.4. block diagram of the second order PLL using single-pole loop filter.

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-419]

LOOP LOCK-RANGE & CAPTURE RANGE

The loop lock-range is represented as the range of frequency about ω_o for which PLL maintains the relationship

$$\omega_i = \omega_{osc}$$

If the phase detector can determine the phase difference between θ_i & θ_{osc}

Over a $\pm \frac{\pi}{2}$ range, then the lock-range is defined as

$$\begin{aligned} \omega_L &= \pm \Delta \omega_{osc} \\ &= K_d A K_o \left(\pm \frac{\pi}{2} \right) = \pm K_v \left(\frac{\pi}{2} \right) \end{aligned}$$

The capture range is the range of i/p frequencies with in which a initially unlocked loop will get locked with an i/p signal. When $F(s)=1$, the capture range equals the lock-range. If $F(S) = \frac{1}{1+S/\omega_i}$, then the capture range is smaller than the lock-range.