Power Dissipation

Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1.

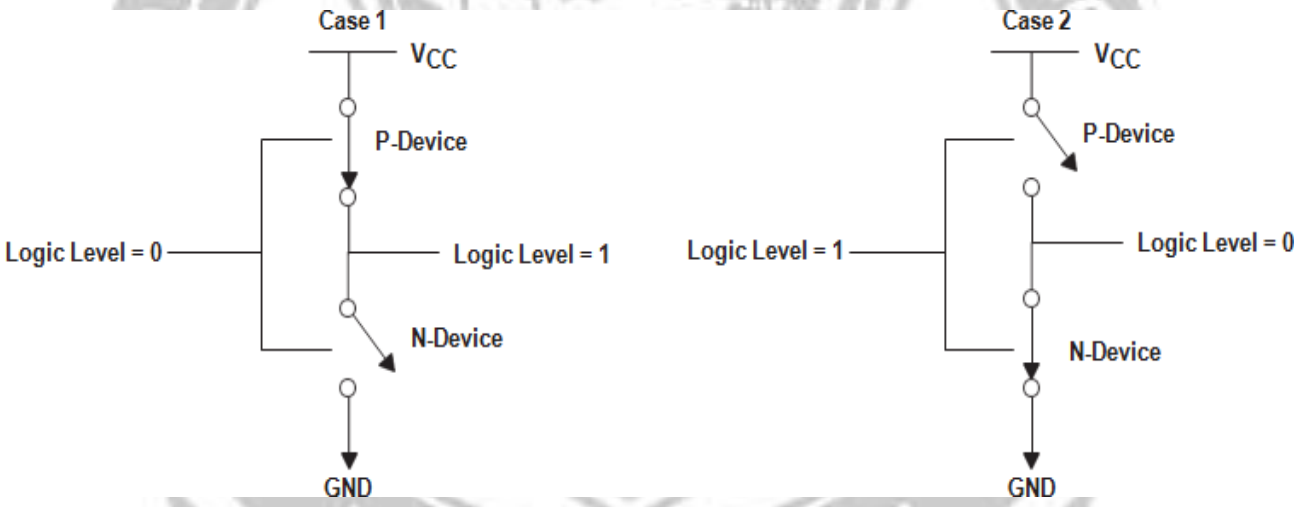


Figure 2.5.1: CMOS Inverter Mode for Static Power Consumption

[Source :Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

As shown in Figure 1, if the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is V_{CC}, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from V_{CC} to GND, the resultant quiescent (steady-state) current is

zero, hence, static power consumption (P_q) is zero.

However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Figure 2.

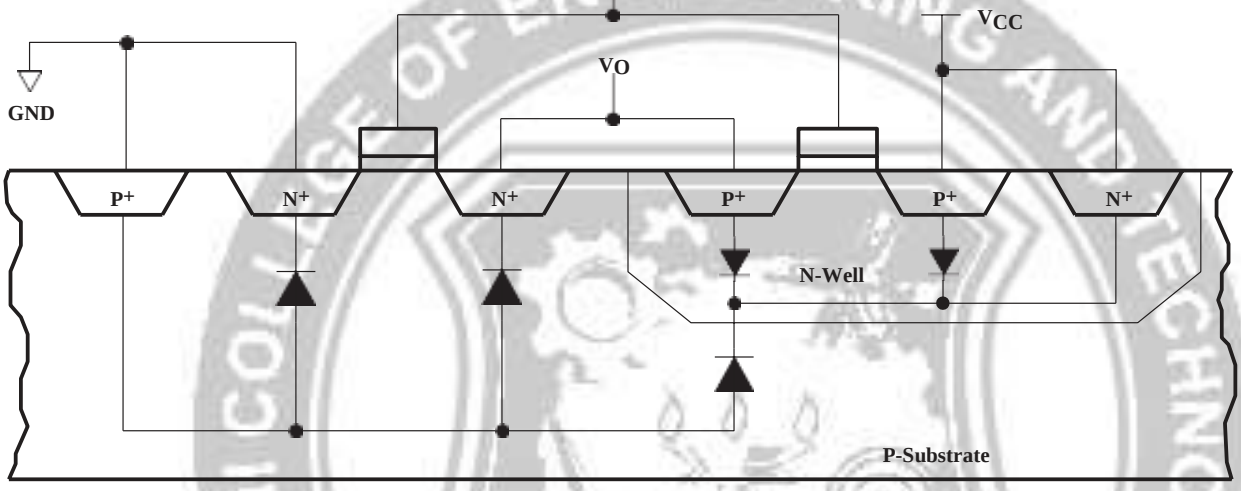


Figure 2.5.2: Model Describing Parasitic Diodes Present in CMOS Inverter

[Source :Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

The source drain diffusion and N-well diffusion form parasitic diodes. In Figure 2, the parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption. The leakage current (I_{lkg})of the diode is described by the following equation:

$$I_{lkg} \text{ is } e^{qV\ kT} \quad 1$$

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation

The leakage current I_{CC} (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or P_S, and can be calculated by equation 3.

$$\mathbf{P_S = V_{CC} \times I_{CC}} \quad \textbf{(3)}$$

V_{CC} =supply voltage

I_{CC} = current into a device (sum of leakage currents as in equation 2)

Another source of static current is I_{CC}. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (P_T), and capacitive-load power consumption (P_L).

Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (*switching current*) plus the *through current* (current that flows from V_{CC} to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the

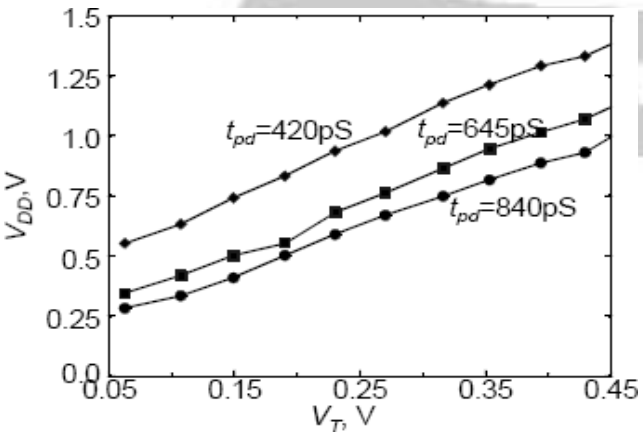
CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance (C_{pd}) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. C_{pd} is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, C_{pd} can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). C_{pd} is discussed in greater detail in the next section.

static and dynamic power dissipation

Low Power Design Principles

The supply voltage for CMOS processes will continue to drop over the coming decade, and may go as low as 0.6V by 2010. To maintain performance under those conditions, it is essential that the device thresholds scale as well.

Figure a shows a plot of the (*VT, VDD*) ratio required to maintain a given performance level (assuming that other device characteristics remain identical). This trade-off is not without penalty. Reducing the threshold voltage, increases the subthreshold leakage current exponentially .



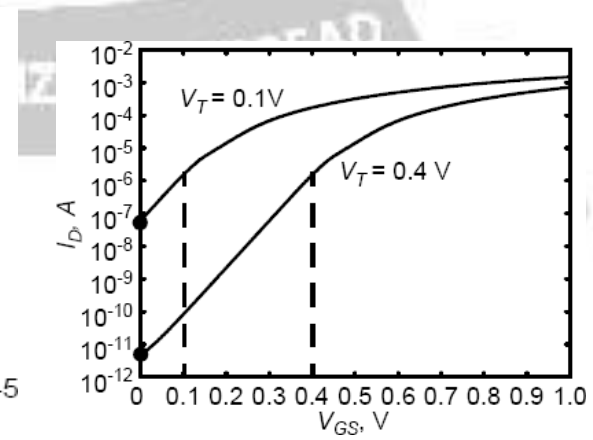


Figure:2.5.3 Voltage Scaling (*VDD/VT* on delay and leakage) (a) VDD/VT for fixed performance (b)

[Source :Neil H.E. Weste, David Money Harris ―CMOS VLSI Design: A Circuits and Systems Perspective…]

Leakage as a function of VT

$$I_{leakage} = I_S 10^{\frac{V_{GS}-V_{Th}}{S}}\left(1 - 10^{-\frac{nV_{DS}}{S}}\right)$$

with *S* the *slope factor* of the device. The subthreshold leakage of an inverter is the current of the NMOS for *Vin* = 0V and *Vout = VDD* (or the PMOS current for *Vin* = *VDD* and *Vout* = 0).

The exponential increase in inverter leakage for decreasing thresholds illustrated in Figure b.

These leakage currents are particularly a concern for designs that feature intermittent computational activity separated by long periods of inactivity. For example, the processor in a cellular phone remains in idle mode for a majority of the time. While the processor is shutdown mode, the system should ideally consume zero or near-zero power. This is only possible if leakage is low—this is, the devices have a high threshold voltage. This is in contradictory to the scaling scenario that we just depicted, where high performance under low supply voltage means reduced thresholds. To satisfy the contradicting requirements of high-performance during active periods, and low leakage during standby, several process modifications or leakage-control techniques have been introduced in CMOS processes. Most processes with feature sizes at and below 0.18 mm CMOS support devices with different thresholds—typically a device with low threshold for high performance circuits, and a transistor with high threshold for leakage control. Another approach that is gaining ground is the dynamic control of the threshold voltage of a device by exploiting the body effect of the transistor.

To use this approach for the control of individual devices requires a dual-well process.

Clever circuit design can also help to reduce the leakage current, which is a function of the circuit topology and the value of the inputs applied to the gate. Since *VT* depends on body bias (*VBS*), the sub-threshold leakage of an MOS transistor depends not only on the gate drive (*VGS*), but also on the body bias. In an inverter with *In* = 0, the sub-threshold leakage of the inverter is set by the NMOS transistor with its *VGS* = *VBS* = 0 V. In more complex CMOS gates, the leakage current depends upon the input vector. For example, the sub-threshold leakage current of a two-input NAND gate is the least when *A*=*B*=0. Under these conditions, the intermediate node X settles to,

$$V_X \approx V_{th} \ln(1+n)$$

The NAND gate sub-threshold leakage is then set by the top-most NMOS transistor with *VGS*=*VBS*=-*VX*. Clearly, the sub-threshold leakage under this condition is slightly smaller than that of the inverter. This reduction in sub-threshold leakage due to stacked transistors is called.