3.6 MONOLITHIC PHASE LOCKED LOOPS

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges. IC 565 is available in a 14 pin DIP package and 10 pin metal can package. Figure 3.6.1 shows the 14 pin DIP package of NE/SE 565.

NE/SE 565 PLL Block Diagram is shown in figure 3.6.2.The o/p frequency of the VCO is given by equation $f_o = \frac{0.25}{R_T C_T} HZ$

where R_1&C_1 are an external resistor & a capacitor connected to pins 8 & 9

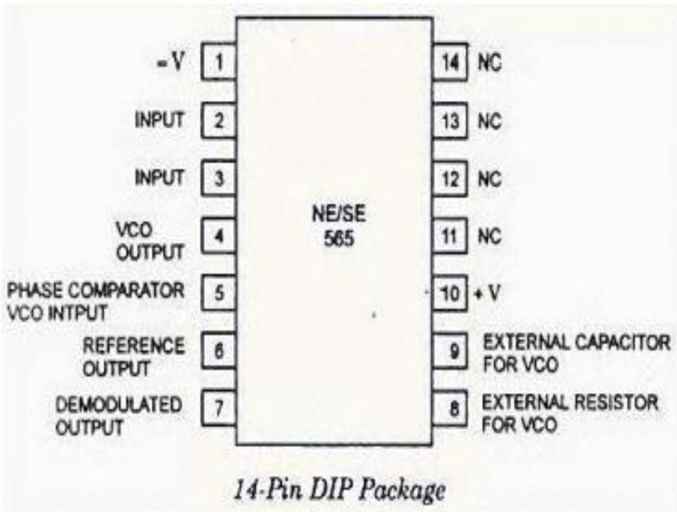

Figure 3.6.1.Pin Configuration of NE/SE565

[source: https://sites.google.com/site/learneasyyourself/home/lic/phase-locked-loop-ic-s]

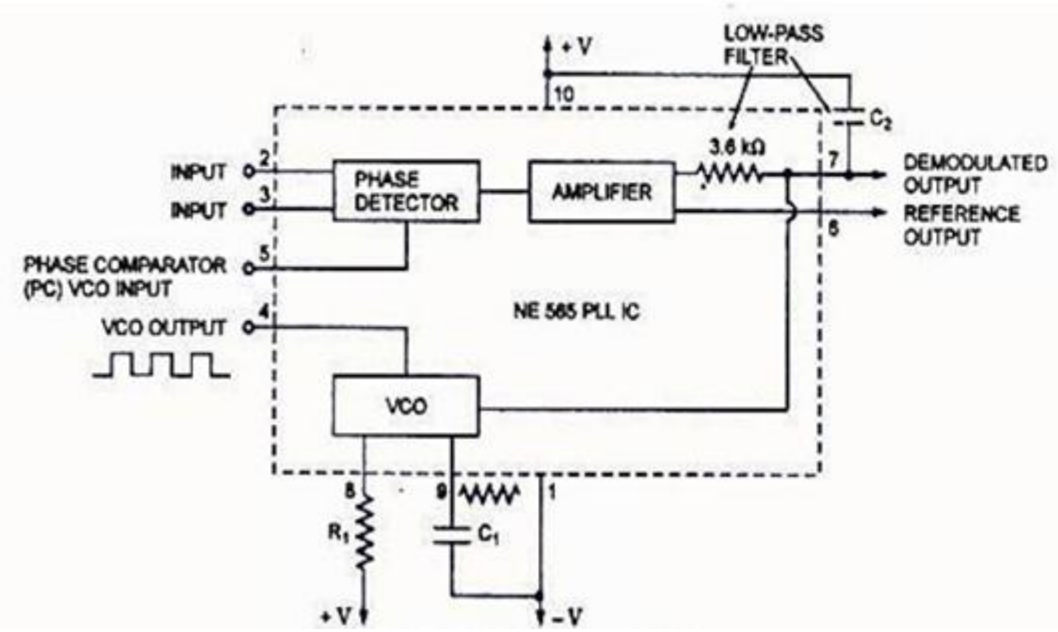

Figure 3.6.2 NE/SE 565 PLL Block Diagram

[source: https://sites.google.com/site/learneasyyourself/home/lic/phase-locked-loop-ic-s]

A value between 2KΩ & 20 KΩ is recommended for R_1.The VCO free running freq is adjusted with R_1 & C_1 be at the centre of the i/p frequency range. A short circuit between pins 4 & 5 connects the VCO o/p to the phase comparator so as to compare f_o with i/p signal f_s.A capacitor C is connected between pin 7 & pin 10 to make a low pass filter with the internal resistance of 3.6 KΩ.The important electrical characteristics of the 565 PLL are, ·

- Operating frequency range: 0.001Hz to 500 Khz. ·
- Operating voltage range: ±6 to ±12v ·
- Input level required for tracking: 10mv rms min to 3 Vpp max ·
- Input impedance: 10 K ohms typically. ·
- Output sink current: 1mA ·
- Output source current: 10 mA

DERIVATION OF LOCK-IN RANGE

If Φ radians- phase difference between the signal & the VCO voltage.The o/p voltage of the analog phase detector is given by

$$V_e = K_\Phi(\Phi - \tfrac{\pi}{2})\text{-----}(1)$$

$where\ K_\Phi$
$\rightarrow phase\ angle\ to\ voltage\ transfer\ coefficient\ of\ the\ phase\ detector.$

The o/p voltage of VCO is

$$V_c = AK_\Phi(\Phi - \tfrac{\pi}{2})\text{-------}(2)$$

$$where\ A \rightarrow voltage\ gain\ of\ the\ amplifier$$

This V_c shifts VCO frequency from its free running frequency f_o to a frequency f given by

$$f = f_o + K_v V_c\text{---}(3)$$

Where K_v—voltage to freq transfer coefficient of the VCO

When PLL is locked in to signal frequency f_s

$$f = f_s = f_o + K_v V_c$$

$$f_s - f_o = K_v V_c$$

$comparing\ (4)\&\ (2)$

$$\frac{(f_s - f_o)}{KV} = AK_\Phi(\Phi - \frac{\pi}{2})$$

$$\left(\Phi - \frac{\pi}{2}\right) = \frac{(f_s - f_o)}{KVAK_\Phi}$$

$$(\Phi) = \frac{\pi}{2} + \frac{(f_s - f_o)}{KVAK_\Phi}\ \text{----}(5)$$

Max o/p voltage magnitude available from the phase detector occurs for Φ=$\boldsymbol{\pi}$ & 0 radians.

$$(1)\rightarrow V_{e(max)} = \pm K_\Phi \frac{\pi}{2}$$

The corresponding value of the max control voltage available to drive VCO will be

$$(2)\rightarrow V_{c(max)} = \pm A K_{\Phi} \frac{\pi}{2}$$

The max VCO frequency swing that can be obtained is given by

$$(3) \rightarrow (f - f_o)_{max} = K_V V_{C(max)}$$

$$(f - f_o)_{max} = K_V A K_{\Phi} \frac{\pi}{2}$$

The max range of signal frequencies over which PLL can remain locked will be

$$f_s = f_o \pm (f - f_o)_{max}$$

$$f_s = f_o \pm K_V A K_{\Phi} \frac{\pi}{2}$$

$$f_s = f_o \pm \Delta f_L$$

Lock –in Range

$$\Delta f_L = \pm K_V A K_{\Phi} \frac{\pi}{2}$$

$$2\Delta f_L = \pm K_V A K_{\Phi} \boldsymbol{\pi}$$

$$w.k.t,\ K_v = \frac{8 f_o}{V}$$

$$V = +V_{cc} - (-V_{cc})$$

$$K_{\Phi} = \frac{1.4}{\pi}$$

A=1.4

$$lock - in\ range\ \Delta f_L = \pm \frac{8 f_o}{V}\ \ X \frac{1.4}{\pi} X 1.4 X \boldsymbol{\pi}$$

$$\Delta f_L = \pm \frac{7.8 f_o}{V}$$

DERIVATION OF CAPTURE RANGE

When PLL is not locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal & the VCO o/p voltage

$$\Phi = (w_s t + \theta_s) - (w_o t + \theta_o)$$

$$\Phi = (w_s t) - (w_o t) + (\theta_s - \theta_o)$$

$$\Phi = (w_s - w_o)t + \Delta\theta$$

The phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\Phi}{dt} = w_s - w_0$$

The phase detector o/p voltage will not have a dc component but will produces on ac voltage with a triangular waveform of peak amplitude $(K_\Phi \frac{\pi}{2})$ & a fundamental frequency

$$(f_s - f_o) = \Delta f$$

LPF is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j\frac{f}{f_1}}$$

$$f_1 = \frac{1}{2\pi RC}$$

$$(\frac{f}{f_1})^2 \gg 1 \; then \; T(f) = \frac{1}{j\frac{f}{f_1}}$$

$$T(f) = \frac{f_1}{jf}$$

Fundamental frequency term supplied to LPF by the phase Detector will be the difference frequency

$$\Delta f = f_s - f_o$$

LPF Transfer function will be

$$T(\Delta f) = \frac{f_1}{\Delta f}$$

$$T(\Delta f) = \frac{f_1}{f_s - f_o}$$

Voltage V_c to drive the VCO is

$$V_c = V_e \; X \; T(f) \; X \; A$$

$$V_{c(max)} = V_{e(max)} \; X \; T(f) \; X \; A$$

$$= \pm K_\Phi \frac{\pi}{2} A(\frac{f_1}{\Delta f})$$

Then the corresponding value of the max VCO frequency shift is

$$(f - f_o)_{max} = K_v V_{c(max)}$$

$$= \pm K_v K_\Phi \frac{\pi}{2} A(\frac{f_1}{\Delta f})$$

Sub $f = f_s$→max signal freq range that can be acquired by PLL is

$$(f_s - f_o)_{max} = \pm K_v K_\Phi \frac{\pi}{2} A(\frac{f_1}{\Delta f_c})$$

Now, $\Delta f_c = (f_s - f_o)_{max}$

$$\Delta f_c = \pm K_v K_\Phi \frac{\pi}{2} A(\frac{f_1}{\Delta f_c})$$

$$\Delta f_c{}^2 = K_v K_\Phi \frac{\pi}{2} A f_1$$

$$where, \Delta f_L = \pm K_v K_\Phi \frac{\pi}{2} A$$

$$\Delta f_c{}^2 = f_1 \Delta f_L$$

$$\Delta f_c = \pm\sqrt{f_1 \Delta f_L}$$

The total capture range is

$$2\Delta f_c = 2\sqrt{f_1 \Delta f_L}$$

$$f_1 = \frac{1}{2\pi RC}$$

IC PLL 565, R=3.6KΩ

Capture range is $\pm 2[\frac{\Delta f_L}{2\pi(3.6X10^3)C}]^{\frac{1}{2}}$,Where C→farads