1.2. ENERGY BAND DIAGRAM

The region on the left is p-type with an acceptor density Na, while the region on the right is n-type with a donor density Nd. The dopants are assumed to be shallow, so that the electron (hole) density in the n-type (p-type) region is approximately equal to the donor (acceptor) density.

Thermal equilibrium

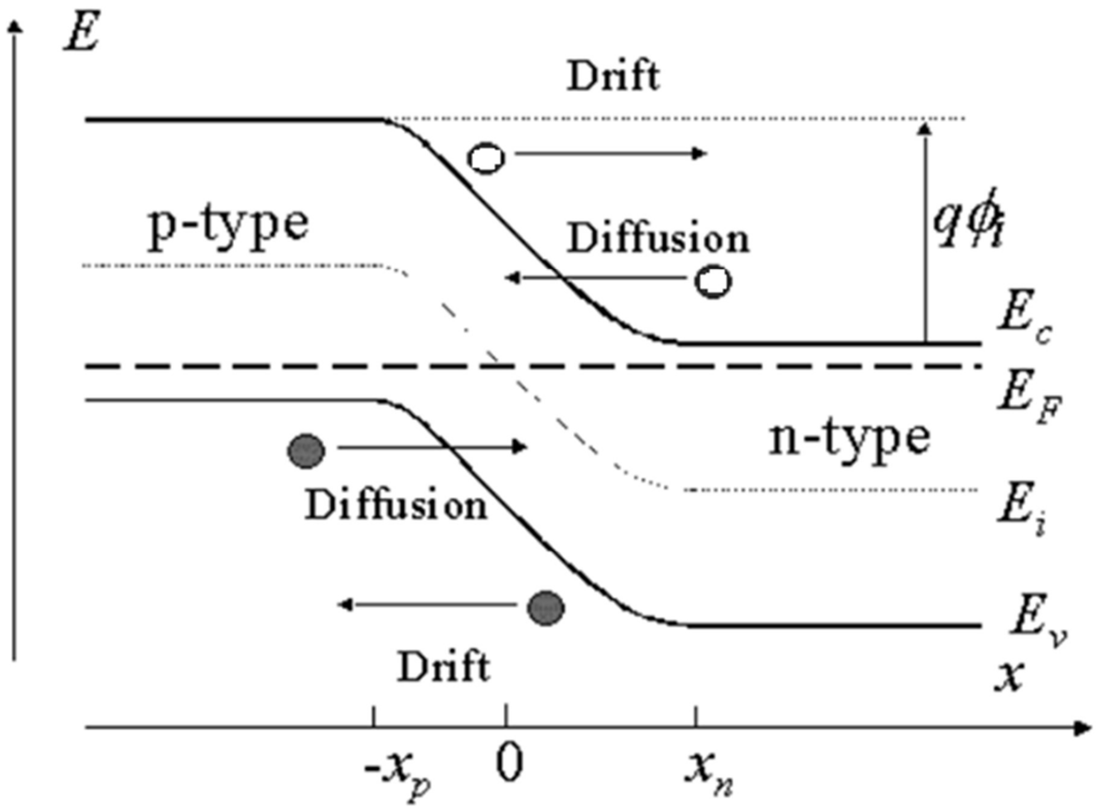

Fig:1.2.1 PN Diode Energy Band Diagram

(Source :https://ecee.colorado.edu)

To reach thermal equilibrium, electrons/holes close to the metallurgical junction diffuse across the junction into the p-type/n-type region where hardly any electrons/holes are present. This process leaves the ionized donors (acceptors) behind, creating a region around the junction, which is depleted of mobile carriers. This region the depletion region, extending from x = -xp to x = xn. The charge due to the ionized donors and acceptors causes an electric field, which in turn causes a drift of carriers in the opposite direction. The diffusion of carriers continues until the drift current balances the diffusion current, thereby reaching thermal equilibrium as indicated by a constant Fermi energy.

While in thermal equilibrium no external voltage is applied between the n-type and p-type material, there is an internal potential, which is caused by the work function difference between the n-type and p-type semiconductors.

Energy band diagram of a p-n junction under reverse and forward bias

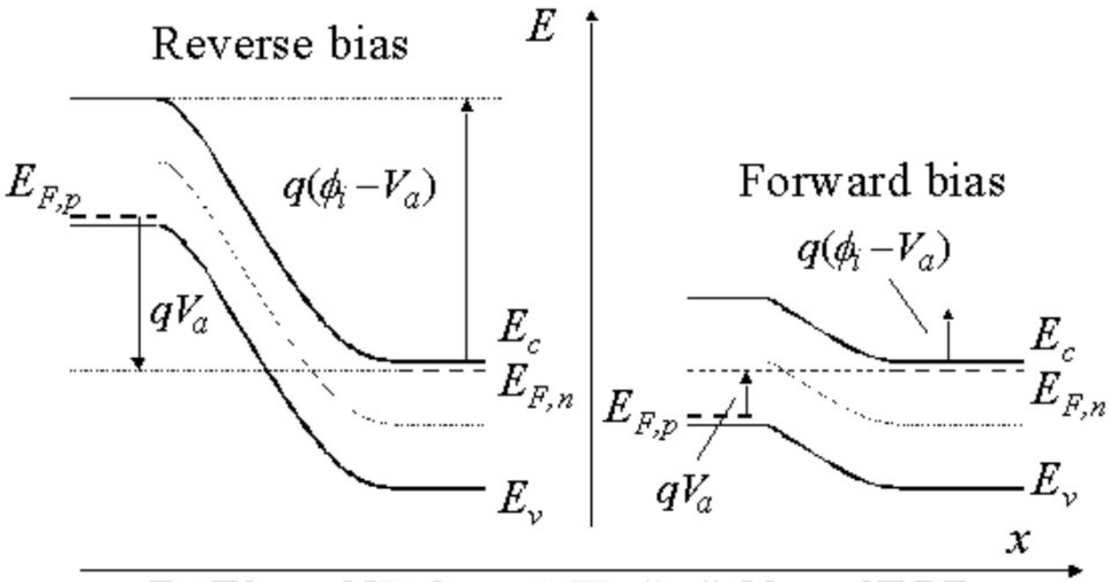

Fig:1.2.2 PN Diode Energy Band Diagram F.B & R.B

(Source :https://ecee.colorado.edu)

P-N diode with an applied bias voltage, Va. A forward bias corresponds to applying a positive voltage to the anode (the p-type region) relative to the cathode (the n-type region). A reverse bias corresponds to a negative voltage applied to the cathode. The applied voltage is proportional to the difference between the Fermi energy in the n-type and p-type quasi-neutral regions.

As a negative voltage is applied, the potential across the semiconductor increases and so does the depletion layer width. As a positive voltage is applied, the potential across the semiconductor decreases and with it the depletion layer width. The total potential across the semiconductor equals the built-in potential minus the applied voltage.