1.6 TIMING DIAGRAM

The machine cycles are the basic operations performed by the processor, while instructions are executed. The time taken for performing each machine cycle is expressed in terms of T-states.

Timing Diagram is a graphical representation of the execution of an instruction by a processor.The execution time is represented in T-states. One T-state is the time period of one clock cycle of the microprocessor.

Parts of an instruction

Instruction:-

- It is a command which direct the processor to execute certain task.
  Ex:- MOV A,B

Operator:

- what operation the MP will perform.
  Ex:-MOV

Operand:-

- The source of data on which instruction is to be operated
  Ex:- A,B

Classification of instruction based on byte length

- 1 byte instruction
- 2 byte instruction
- 3 byte instruction

Instruction Cycle

- The time required to execute an instruction is called instruction cycle.

Machine Cycle

- The time required to access the memory or input/output devices is called machine cycle.

T-State

- It is the time corresponding to one clock period.
- A portion of an operation carried out in one system clock period is called as T-state.

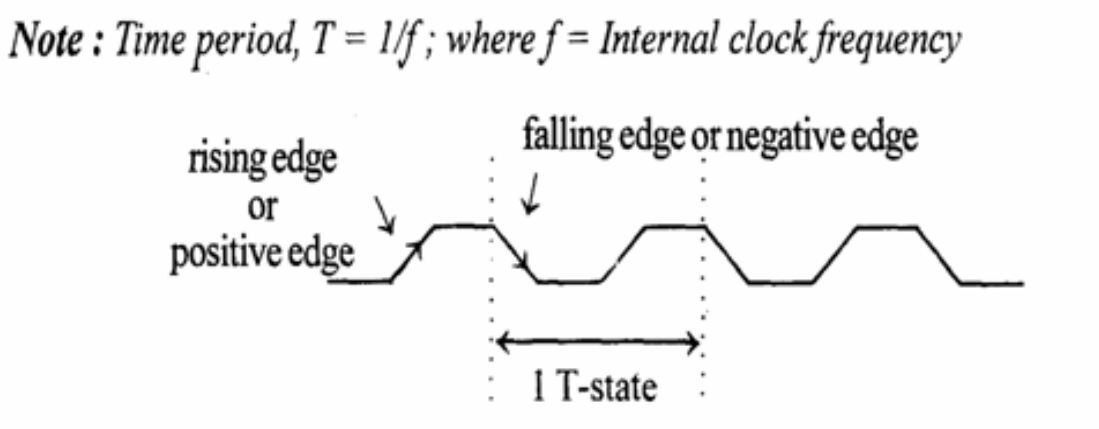

Figure 1.6.1 T-State

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-65]

Machine Cycles of 8085

The 8085 microprocessor has 5 basic machine cycles. They are,

- Opcode fetch cycle (4T)
- Memory read cycle (3 T)
- Memory write cycle (3 T)
- I/O read cycle (3 T)
- I/O write cycle (3 T)

IO/M	S0	S1	Processor state
High impedance	0	0	Halt
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Op-code fetch
1	0	1	I/O Read
1	1	0	I/O Write
1	1	1	Interrupt acknowledgement

Opcode fetch machine cycle

- Each instruction of the processor has one byte opcode.
- The opcodes are stored in memory. So, the processor executes the opcode fetch machine cycle to fetch the opcode from memory.
- Hence, every instruction starts with opcode fetch machine cycle.
- The time taken by the processor to execute the opcode fetch cycle is 4T.
- In this time, the first, 3T-states are used for fetching the opcode from memory and the remaining T-states are used for decoding. & execution.

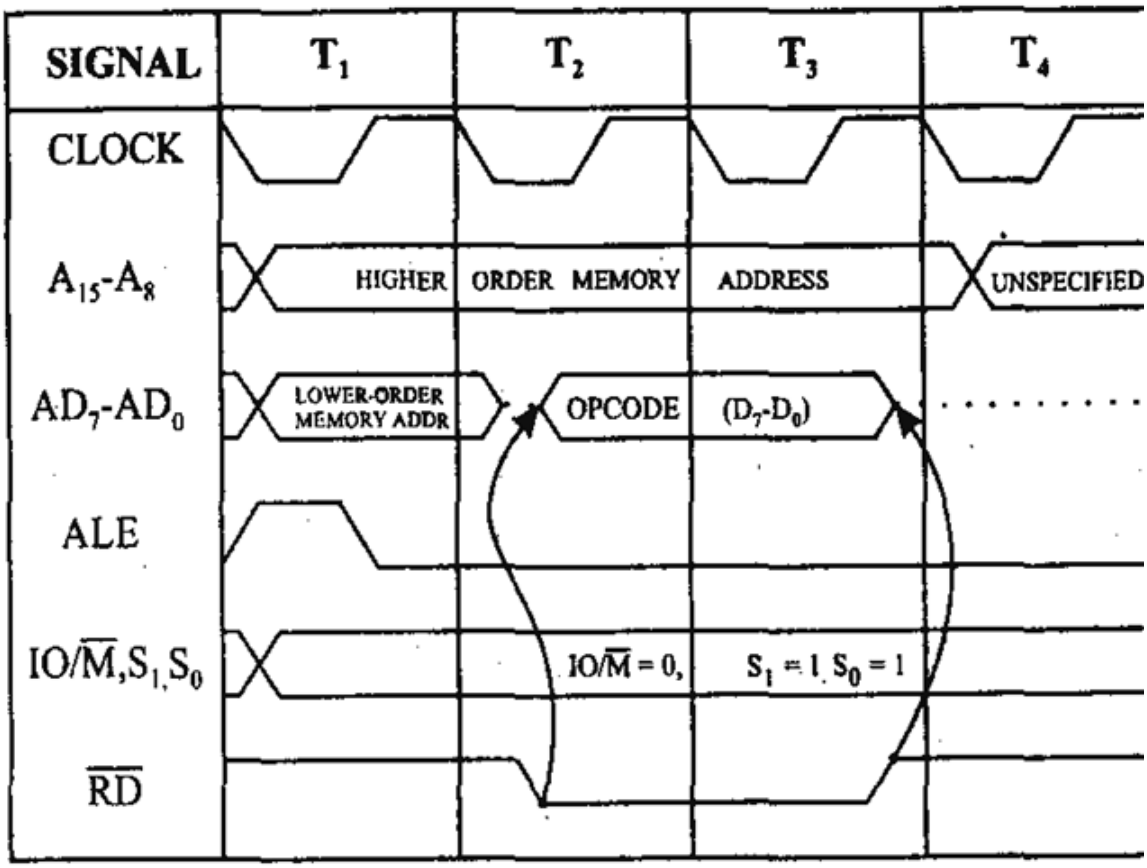

Figure 1.6.2 Opcode fetch machine cycle

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-65]

Memory Read Machine Cycle

- The memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to execute this cycle.
- The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle.

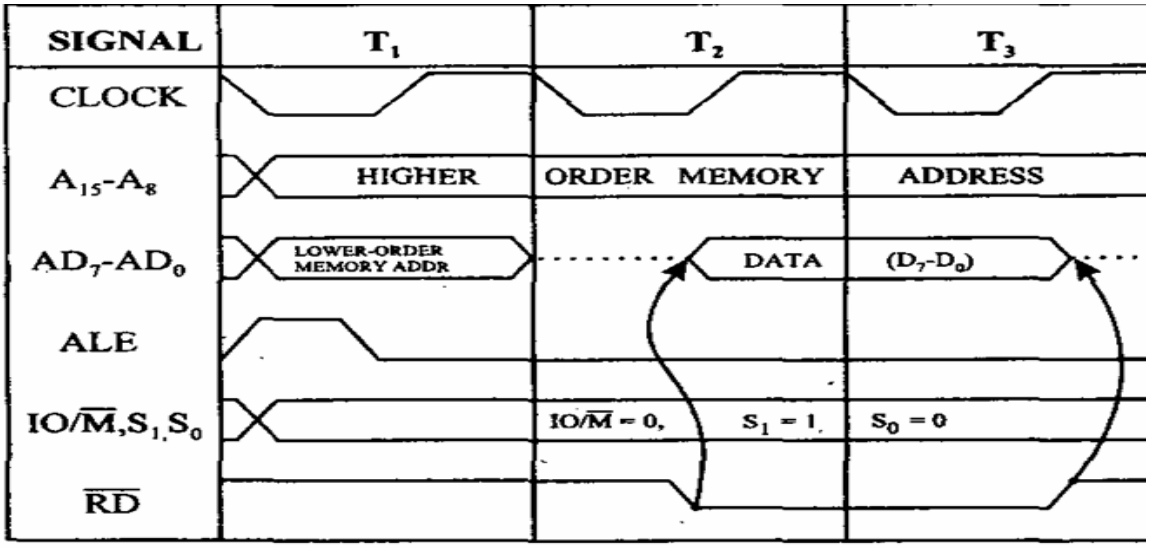

Figure 1.6.3 Memory Read Machine Cycle

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-66]

Memory Write Machine Cycle

- The memory write machine cycle is executed by the processor to write a data byte in a memory location.
- The processor takes, 3T states to execute this machine cycle.
- The 8085 places the address (2065H) on the address bus
- Identifies the operation as a 'memory write' (IO/M=0, s1=0, s0=1).
- Places the contents of the accumulator on the data bus and asserts the signal WR.
- During the last T-state, the contents of the data bus are saved into the memory location.

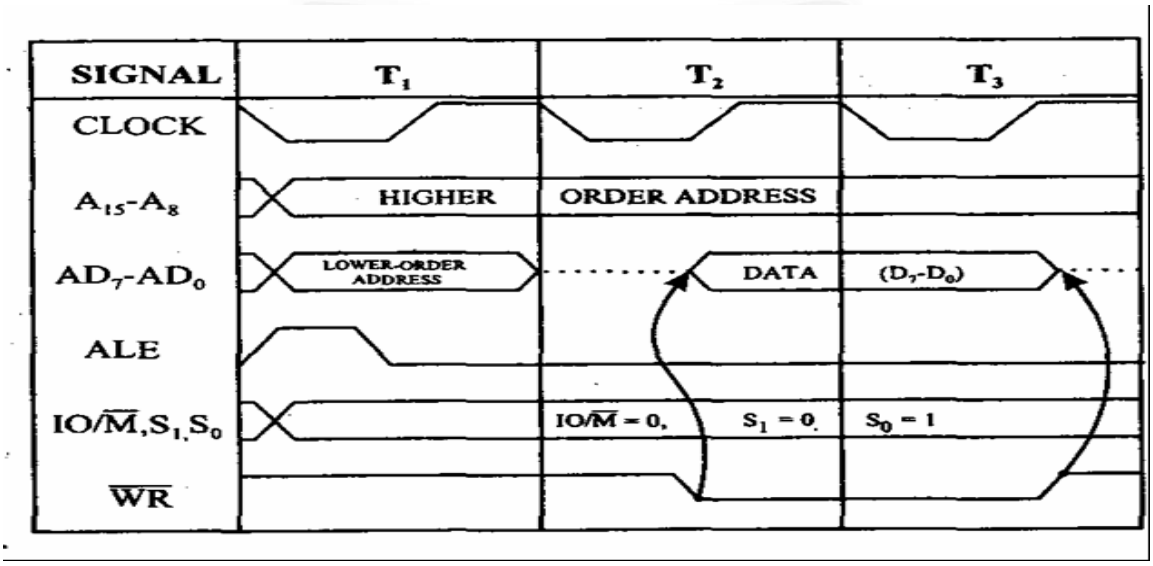

Figure 1.6.4 Memory write Machine Cycle

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-68]

I/O Read Cycle Of 8085

- The I/O Read cycle is executed by the processor to read a data byte from I/O port or from the peripheral.
- The processor takes 3T states to execute this machine cycle.
- The IN instruction uses this machine cycle during the execution.

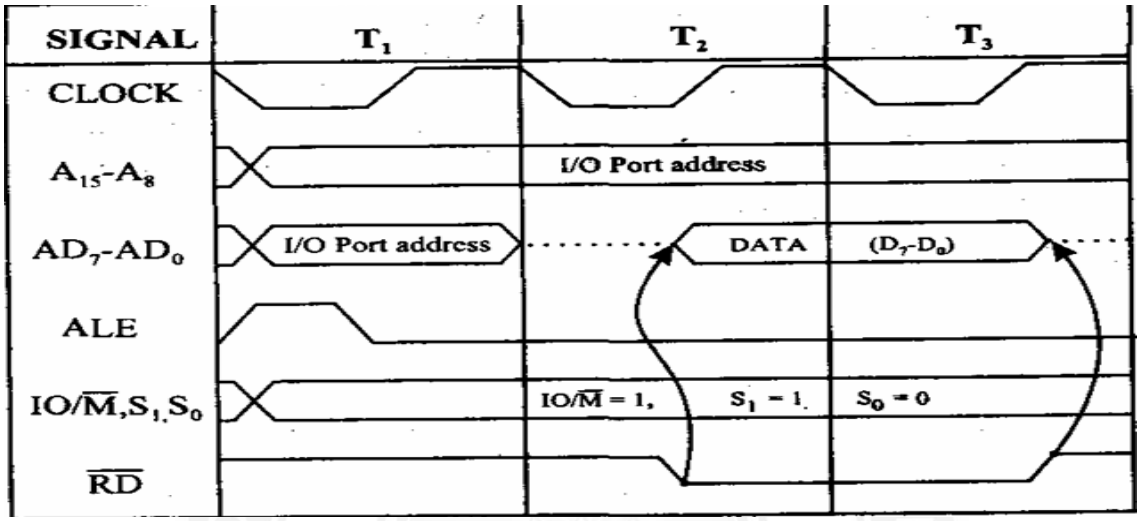

Figure 1.6.5 I/O Read Machine Cycle

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-79]

I/O Write Cycle Of 8085

- The I/O write machine cycle is executed by the processor to write a data byte in the I/O port or to a peripheral, which is I/O, mapped in the system.
- The processor takes, 3T states to execute this machine cycle.

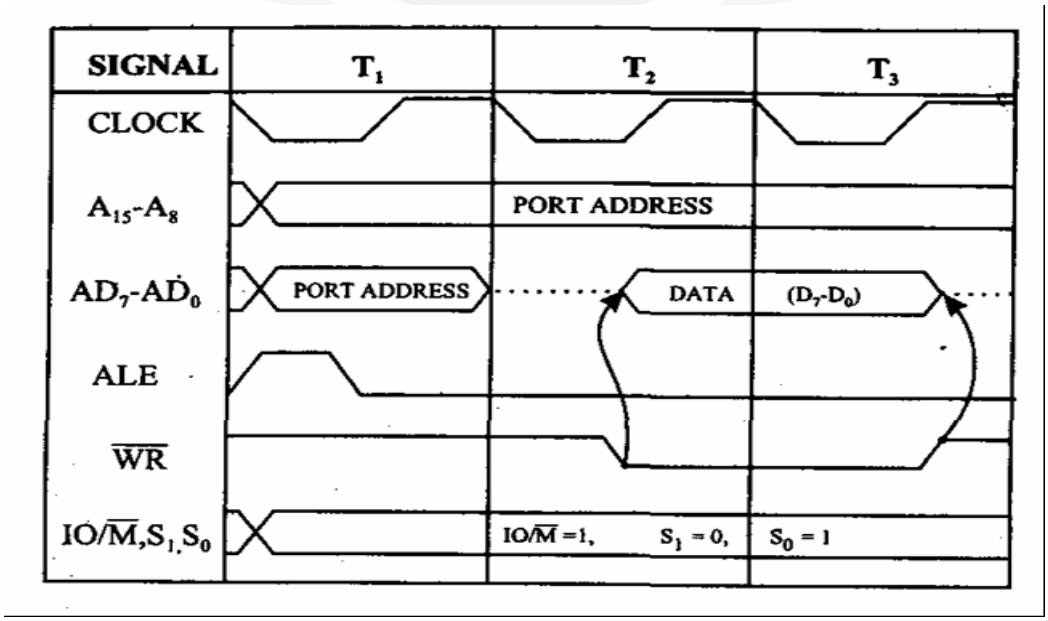

Figure 1.6.5 I/O Write Machine Cycle

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-79]