Dynamic latches

Dynamic Transmission-Gate Based Edge-triggered Registers

A fully dynamic positive edge-triggered register based on the master-slave concept is shown in figure. When CLK = 0, the input data is sampled on storage node 1, which has an equivalent capacitance of C1 consisting of the gate capacitance of I1, the junction capacitance of T1, and the overlap gate capacitance of T1.

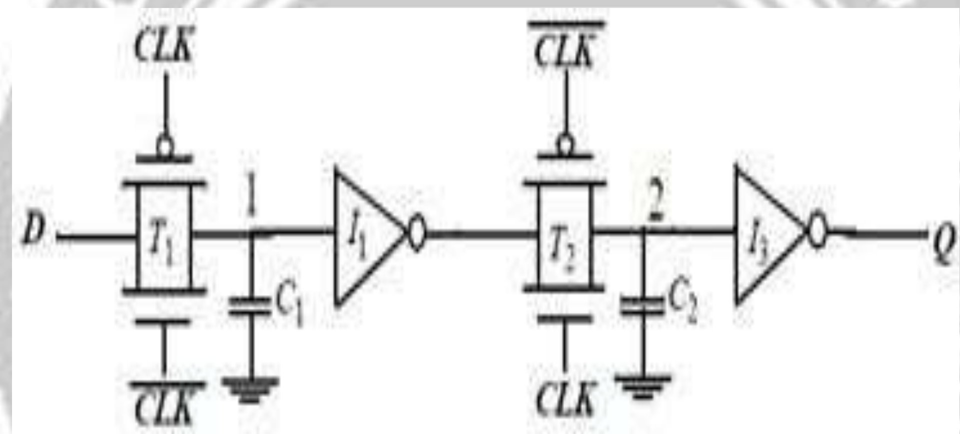

Figure 3.3.1: Dynamic Edge-triggered Registers

[Source : Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective …]

During this period, the slave stage is in a hold mode, with node 2 in a high-impedance (floating) state. On the rising edge of clock, the transmission gate T2 turns on, and the value sampled on node 1 right before the rising edge propagates to the output Q (note that node 1 is stable during the high phase of the clock since the first transmission gate is turned off).

Node 2 now stores the inverted version of node 1. This implementation of an edge- triggered register is very efficient as it requires only 8 transistors.

The sampling switches can be implemented using NMOS-only pass transistors, resulting in an even-simpler 6 transistor implementation. The reduced transistor count is attractive for high-performance and low-power systems.

The set-up time of this circuit is simply the delay of the transmission gate , and corresponds to the time it takes node 1 to sample the D input.The hold time is approximately zero, since the transmission gate is turned off on the clock edge and further inputs changes are ignored. The propagation delay (tc-q) is equal to two inverter delays plus the delay of the transmission gate T2.

One important consideration for such a dynamic register is that the storage nodes (i.e., the state) has to be refreshed at periodic intervals to prevent a loss due to charge leakage, due to diode leakage as well as sub-threshold currents. In datapath circuits, the refresh rate is not an issue since the registers are periodically clocked, and the storage nodes are constantly updated.

Clock overlap is an important concern for this register. Consider the clock waveforms shown in below figure. During the 0-0 overlap period, the NMOS of T1 and the PMOS of T2 are simultaneously on, creating a direct path for data to flow from the D input of the register to the Q output. This is known as race condition. The output Q can change on the falling edge if the overlap period is large

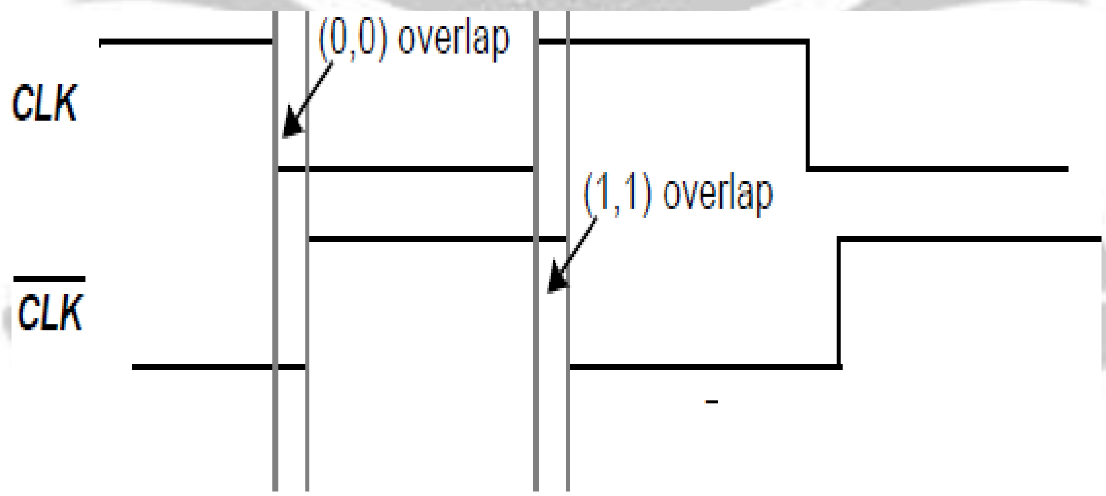

Figure 3.3.2 : Impact of non-overlapping clocks

[Source : Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design …]

CMOS Dynamic Register: A Clock Skew Insensitive Approach

The CMOS Register

The following shows an ingenious positive edge-triggered register based on the master- slave concept which is insensitive to clock overlap. This circuit is called the C2MOS (Clocked CMOS) register. The register operates in two phases.

1. CLK = 0 (CLK = 1):

2. The roles are reversed when CLK = 1:

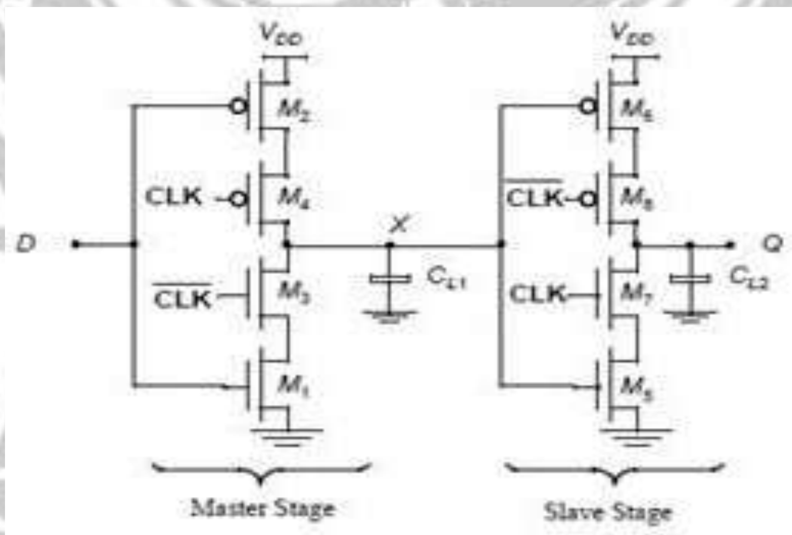

Figure 3.3.3: master slave edge-triggered register

[Source : Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design …]

It can be stated that the C2MOS latch is insensitive to clock overlaps because those overlaps activate either the pull-up or the pull-down networks of the latches, but never both of them simultaneously. If the rise and fall times of the clock are sufficiently slow, however, there exists a time slot where both the NMOS and PMOS transistors are conducting. This creates a path between input and output that can destroy the state of the circuit.

Dual-edge Triggered Registers

So far, we have focused on edge-triggered registers that sample the input data on only one of the clock edges (rising or falling). It is also possible to design sequential circuits that sample the input on both edges. The advantage of this scheme is that a lower frequency clock (half of the original rate) is distributed for the same functional throughput, resulting in power savings in the clock distribution network.

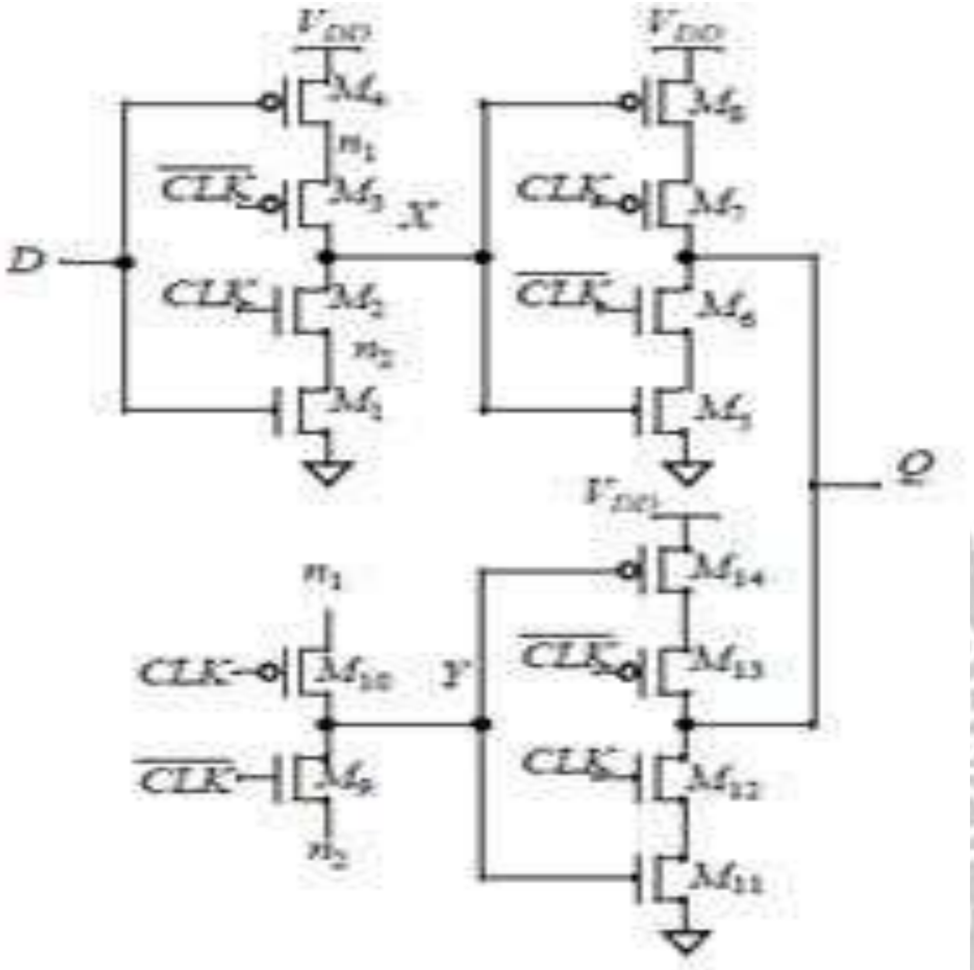

Figure 3.3.4: CMOS based dual-edge triggered register.

[Source : Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design …]

…

The above figure shows a modification of the C2MOS register to enable sampling on both edges.

True Single-Phase Clocked Register (TSPCR)

In the two-phase clocking schemes described above, care must be taken in routing the two clock signals to ensure that overlap is minimized. While the C2MOS provides a skew- tolerant solution, it is possible to design registers that only use a single phase clock. The basic single-phase positive and negative latches are shown in figure.

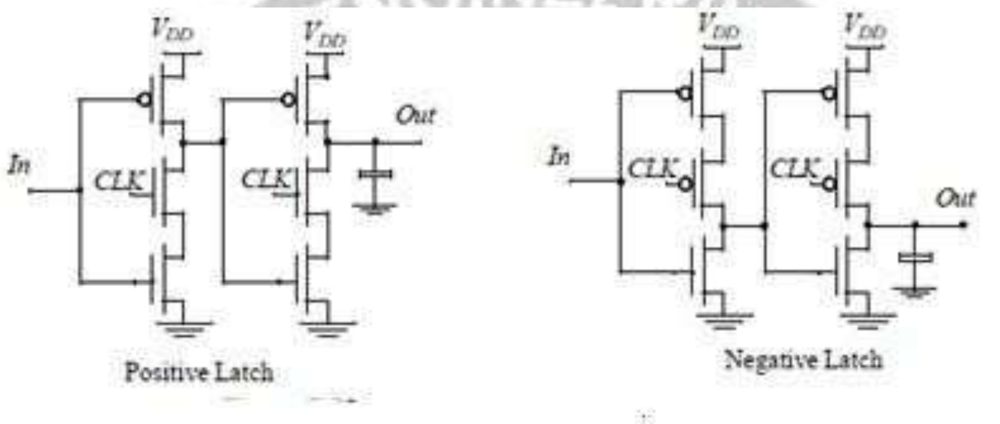

Fig 3.3.5: True Single-Phase Clocked Register

[Source : Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design …]

For the positive latch, when CLK is high, the latch is in the transparent mode and corresponds to two inverters; the latch is non-inverting, and propagates the input to the output. On the other hand, when C LK = 0, both inverters are disabled, and the latch is in hold- mode. Only the pull-up networks are still active, while the pull-down circuits are deactivated. As a result of the dual-stage approach, no signal can ever propagate from the input of the latch to the output in this mode. A register can be constructed by positive and negative latches.

Synchronous Timing:

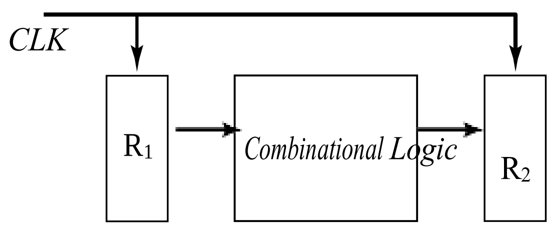

Fig 3.3.6: Synchronous Timing

[Source : Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design …]

The following timing parameters characterize the timing of the sequential circuit.

- The contamination (minimum) delay $t_{c-q,cd}$, and maximum propagation delay of the register t_{c-q}.
- The set-up (t_{su}) and hold time (t_{hold}) for the registers.
- The contamination delay $t_{logic,cd}$ and maximum delay t_{logic} of the combinational logic.
- t_{clk1} and t_{clk2}, corresponding to the position of the rising edge of the clock relative to a global reference.

Clock Non idealities:

Clock skew

✓ Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}

Clock jitter

✓ Temporal variations in consecutive edges of the clock signal; modulation + random noise

✓ Cycle-to-cycle (short-term) t_{JS} Long term t_{JL}

Variation of the pulse width

✓ Important for level sensitive clocking

Clock Skew and Jitter:

✓ Both skew and jitter affect the effective cycle time

✓ Only skew affects the race margin

Sources of Skew and Jitter:

- **Clock-Signal Generation-** The generation of the clock signal itself causes jitter
- **Manufacturing Device Variations**
- **Interconnect Variations-**One important source of interconnect variation is the Inter-level Dielectric (ILD) thickness variations.
- **Environmental Variations-**Environmental variations are probably the most significant and primarily contribute to skew and jitter. The two major sources of environmental variations are temperature and power supply. Power supply variations is the major source of jitter in clock distribution networks.
- **Capacitive Coupling-**The variation in capacitive load also contributes to timing uncertainty. There are two major sources of capacitive load variations: coupling

between the clock lines and adjacent signal wires and variation in gate capacitance.

Clock-Distribution Techniques:

It is necessary to design a clock network that minimizes skew and jitter. Another important consideration in clock distribution is the power dissipation.

Fabrics for clocking-one common approach to distributing a clock are to use balanced paths (or called trees). The most common type of clock primitive is the H-tree network (named for the physical structure of the network) .

In this scheme, the clock is routed to a central point on the chip and balanced paths, that include both matched interconnect as well as buffers, are used to distribute the reference to various leaf nodes. Ideally, if each path is balanced, the clock skew is zero.

- variation in gate capacitance.

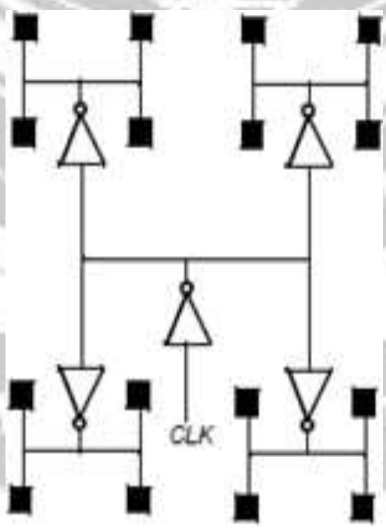

Fig 3.3.7: Example of H-tree clock distribution

[Source : Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective …]

That is, though it might take multiple clock cycles for a signal to propagate from the central point to each leaf node, the arrival times are equal at every leaf node.