

2.8 DECODER

Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of 'n' input variables lines, when it is enabled.

2 to 4 Decoder

Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3 , Y_2 , Y_1 & Y_0 . The block diagram of 2 to 4 decoder is shown in the following figure.

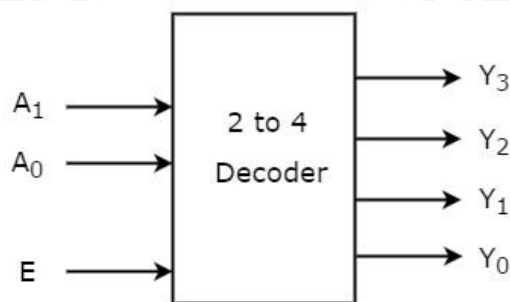


Figure 2.8.1 Block diagram

[Source: https://www.tutorialspoint.com/digital_circuits/digital_circuits_decoders.htm]

One of these four outputs will be '1' for each combination of inputs when enable, E is '1'. The Truth table of 2 to 4 decoder is shown below.

Enable	Inputs		Outputs			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

From Truth table, we can write the Boolean functions for each output as

$$Y_3 = E \cdot A_1 \cdot A_0$$

$$Y_2 = E \cdot A_1 \cdot A_0'$$

$$Y_1 = E \cdot A_1' \cdot A_0$$

$$Y_0 = E \cdot A_1' \cdot A_0'$$

Each output is having one product term. So, there are four product terms in total. We can implement these four product terms by using four AND gates having three inputs each & two inverters. The circuit diagram of 2 to 4 decoder is shown in the following figure.

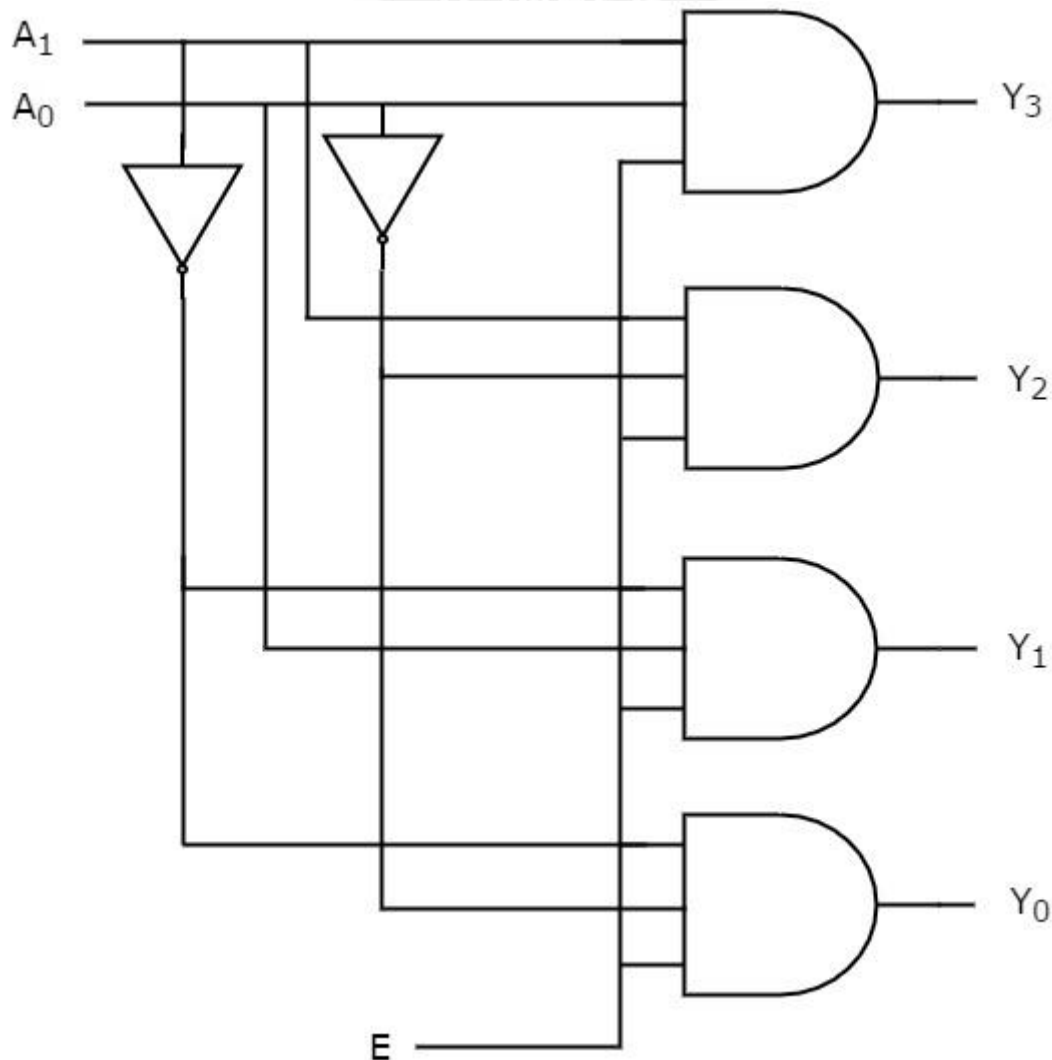


Figure 2.8.2 2 to 4 Decoder

[Source: https://www.tutorialspoint.com/digital_circuits/digital_circuits_decoders.htm]

Therefore, the outputs of 2 to 4 decoder are nothing but the min terms of two input variables A_1 & A_0 , when enable, E is equal to one. If enable, E is zero, then all the outputs of decoder will be equal to zero.

Similarly, 3 to 8 decoder produces eight min terms of three input variables A_2 , A_1 & A_0 and 4 to 16 decoder produces sixteen min terms of four input variables A_3 , A_2 , A_1 & A_0 .

Implementation of Higher-order Decoders

Now, let us implement the following two higher-order decoders using lower-order decoders.

- 3 to 8 decoder
- 4 to 16 decoder

3 to 8 Decoder

In this section, let us implement 3 to 8 decoder using 2 to 4 decoders. We know that 2 to 4 Decoder has two inputs, A_1 & A_0 and four outputs, Y_3 to Y_0 . Whereas, 3 to 8 Decoder has three inputs A_2 , A_1 & A_0 and eight outputs, Y_7 to Y_0 .

We can find the number of lower order decoders required for implementing higher order decoder using the following formula.

$$\text{Required number of lower order decoders} = \frac{m_2}{m_1} \quad \text{Required number of lower order decoders} = \frac{m_2}{m_1}$$

Where,

m_1 is the number of outputs of lower order decoder.

m_2 is the number of outputs of higher order decoder.

Here, $m_1 = 4$ and $m_2 = 8$. Substitute, these two values in the above formula.

$$\text{Required number of 2 to 4 decoders} = \frac{8}{4} = 2 \quad \text{Required number of 2 to 4 decoders} = \frac{8}{4} = 2$$

Therefore, we require two 2 to 4 decoders for implementing one 3 to 8 decoder.

The parallel inputs A_1 & A_0 are applied to each 2 to 4 decoder. The complement of input A_2 is connected to Enable, E of lower 2 to 4 decoder in order to get the outputs, Y_3 to Y_0 . These are the lower four min terms. The input, A_2 is directly connected to Enable, E of upper 2 to 4 decoder in order to get the outputs, Y_7 to Y_4 . These are the higher four min terms.

The block diagram of 3 to 8 decoder using 2 to 4 decoders is shown in the following figure.

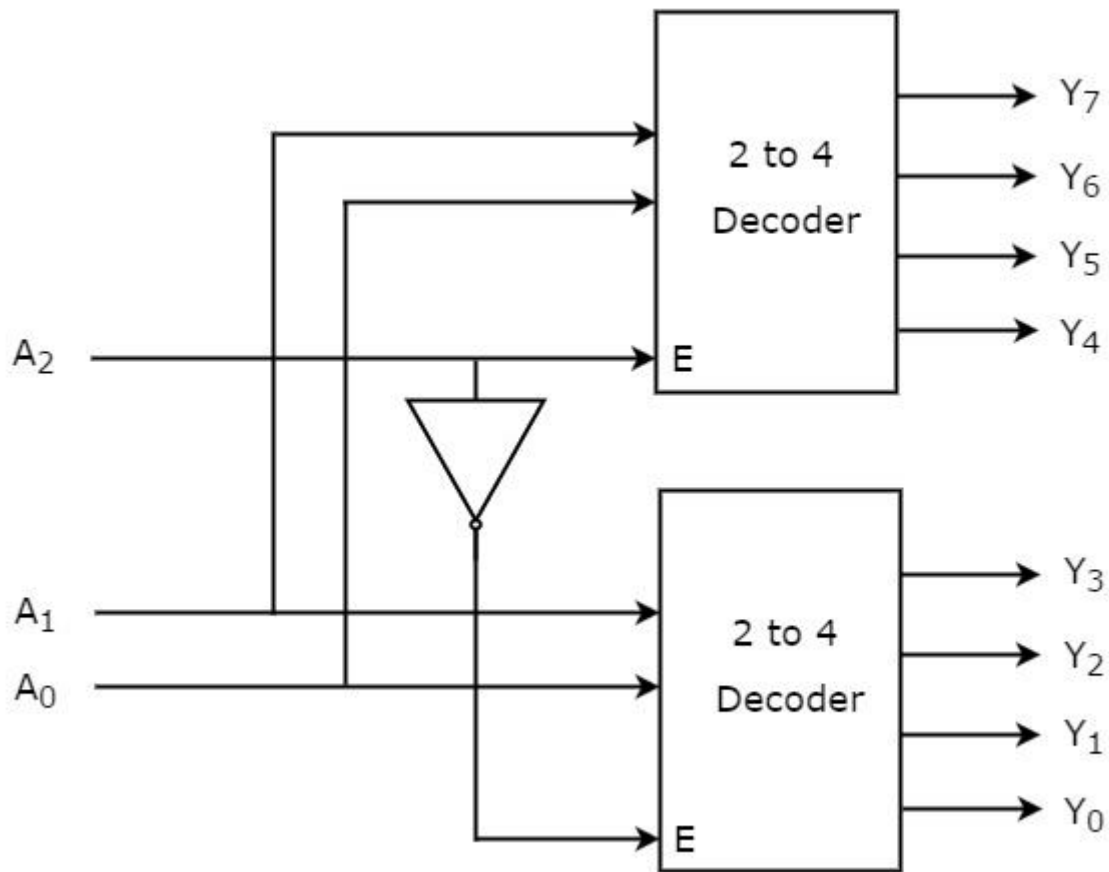


Figure 2.8.3 3 to 8 Decoder

[Source: https://www.tutorialspoint.com/digital_circuits/digital_circuits_decoders.htm]

4 to 16 Decoder

In this section, let us implement 4 to 16 decoder using 3 to 8 decoders. We know that 3 to 8 Decoder has three inputs A_2 , A_1 & A_0 and eight outputs, Y_7 to Y_0 . Whereas, 4 to 16 Decoder has four inputs A_3 , A_2 , A_1 & A_0 and sixteen outputs, Y_{15} to Y_0

We know the following formula for finding the number of lower order decoders required.

$$\text{Required number of lower order decoders} = \frac{m_2}{m_1} \quad \text{Required number of lower order decoders} = \frac{m_2}{m_1}$$

Substitute, $m_1 = 8$ and $m_2 = 16$ in the above formula.

$$\text{Required number of 3 to 8 decoders} = \frac{16}{8} = 2 \quad \text{Required number of 3 to 8 decoders} = \frac{16}{8} = 2$$

Therefore, we require two 3 to 8 decoders for implementing one 4 to 16 decoder.

The block diagram of 4 to 16 decoder using 3 to 8 decoders is shown in the following figure.

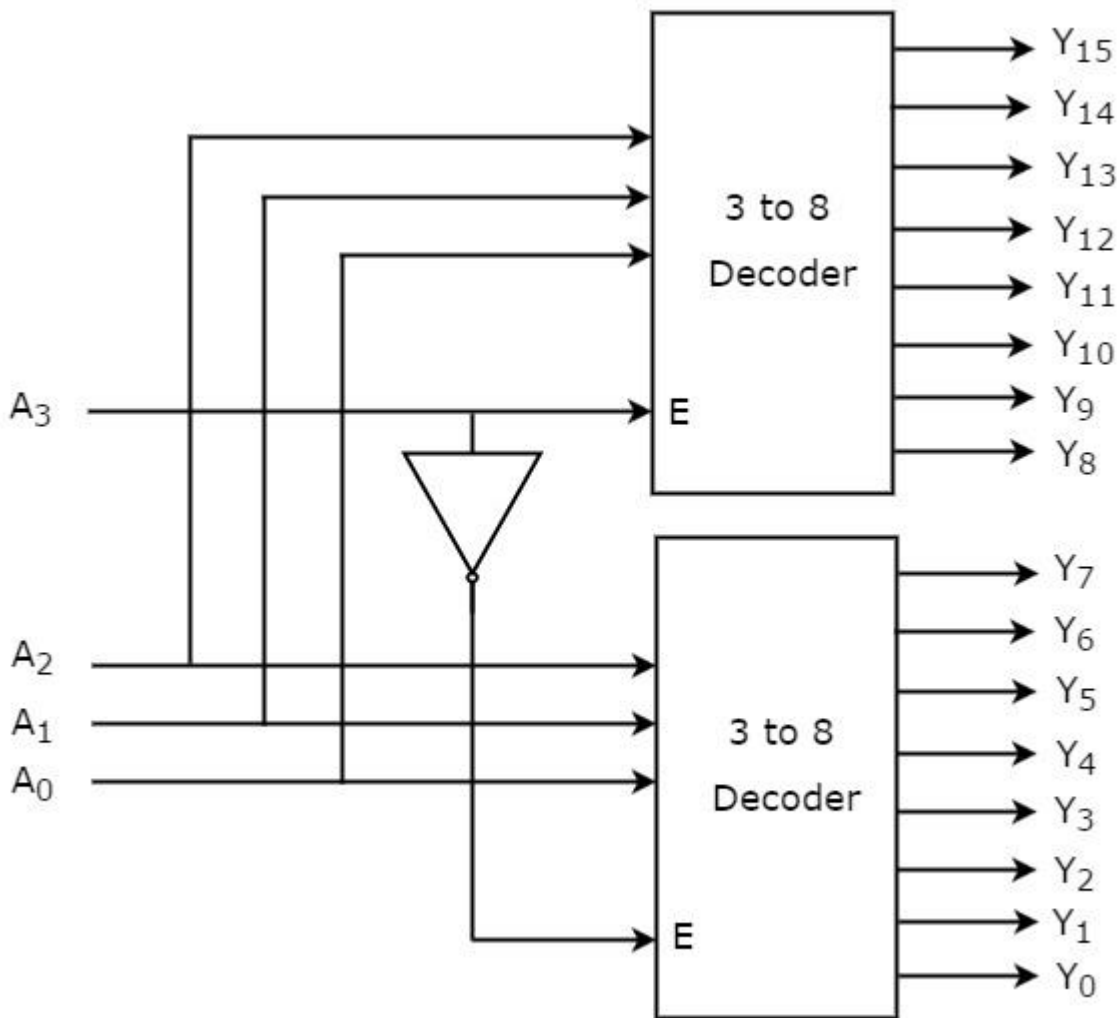


Figure 2.8.4 4 to 16 Decoder

[Source: https://www.tutorialspoint.com/digital_circuits/digital_circuits_decoders.htm]

The parallel inputs A_2 , A_1 & A_0 are applied to each 3 to 8 decoder. The complement of input, A_3 is connected to Enable, E of lower 3 to 8 decoder in order to get the outputs, Y_7 to Y_0 . These are the lower eight min terms. The input, A_3 is directly connected to Enable, E of upper 3 to 8 decoder in order to get the outputs, Y_{15} to Y_8 . These are the higher eight min terms.