

ROHINI COLLEGE OF ENGINEERING AND TECHNOLOGY

(AUTONOMOUS)

(Anjugramam-Kanyakumari Main Road, Palkulam, Variyoor P.O.-629 401, K.K.Dist.)

Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai

Accredited with A+ Grade by NAAC



M.E. EMBEDDED SYSTEM TECHNOLOGIES

(M.E.EEE)

Curriculum & Syllabus

(2024-2025 Admitted Students Onwards)

Vision Statement of RCET

To be an academic institute of continuous excellence towards education and research in rural regime and provide service to nation in terms of nurturing potentially higher social, ethical and engineering companion graduands.

Mission Statement of RCET

- To foster and promote technically competent graduands by imparting the state of art Engineering education in rural regime.
- To enunciate research assisted scientific learning by dissemination of knowledge towards science, agriculture, industry and national security.

Vision of the Department

To create technically competent technocrats to meet the demand of Electrical and Electronics industry and societal need for the wellbeing of human kinds.

Mission of the Department

- To provide knowledge and skills necessary for professional development in Electrical and Electronics Engineering.
- To promote research and creativity in the area of Electrical and Electronics Engineering.
- To promote team work and professional conduct in societal activities.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1 Graduates of the programme will possess career in electrical and allied fields.

PEO2 Graduates will have the ability to adapt to the growing technological requirement of the society through lifelong learning and team work.

PEO3 Graduates of the programme will possess knowledge to pursue higher studies.

PROGRAM OUTCOMES (POs)

PO1 An ability to independently carry out research /investigation and development work to solve practical problems.

PO2 An ability to write and present a substantial technical report/document.

PO3 Students should be able to demonstrate a degree of mastery in Embedded System Technologies. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1 Ability to design and analyze various issues in power system, control and Instrumentation systems and power electronic and drive system.

PSO2 Ability to design and simulate real time problems in electrical system using modern software tools.

PSO3 Ability to apply the knowledge for the development of renewable energy to meet the demand of society.

CREDIT INFO		
Sl.No	Category	Credits
1	Foundation Courses (FC)	4
2	Professional Core Courses (PCC)	35
3	Research Methodology And Ipr Courses (RMC)	2
4	Professional Elective Courses (PEC)	12
5	Employability Enhancement Courses (EEC)	18
6	Open Electives Courses (OEC)	3
7	Audit Courses (AC)	-
Total Credits		74

Foundation Courses (FC)							
Sl.no	Course Code	Course Title	Course Type	L	T	P	Credit
1.	24ES101	Applied Mathematics for Embedded Systems Technologists	FC	3	1	0	4
Professional Core Courses (PCC)							
Sl.no	Course Code	Course Title	Course Type	L	T	P	Credit
1.	24ES102	Design of Embedded Systems	PCC	3	0	0	3
2.	24ES103	Embedded System Networks	PCC	3	0	0	3
3.	24ES104	Microcontroller Based System Design	PCC	3	0	0	3
4.	24ES105	VLSI Design and Reconfigurable Architecture	PCC	3	0	0	3
5.	24ES131	Embedded System Laboratory - I	PCC	0	0	4	2
6.	24ES132	Programming and Algorithms Laboratory	PCC	0	0	4	2
7.	24ES201	Real Time Operating System	PCC	3	0	0	3
8.	24ES202	Advanced Digital System Design	PCC	3	0	0	3

9.	24ES203	Embedded Control for Electric Drives	PCC	3	0	0	3
10.	24ES204	IoT for Smart Systems	PCC	3	0	0	3
11.	24ES251	Embedded System Laboratory - II	PCC	0	0	4	2
12.	24ES252	Embedded Programming Laboratory	PCC	0	0	4	2
13.	24ES301	Software for Embedded Systems	PCC	3	0	0	3
Professional Elective Courses (PEC)							
S.No	Course Code	Course Title	Course Type	L	T	P	Credit
1.	24ES205	Wireless And Mobile Communication	PEC	3	0	0	3
2.	24ES206	Virtual Instrumentation	PEC	3	0	0	3
3.	24ES207	Embedded Processor Development	PEC	3	0	0	3
4.	24ES208	Automotive Embedded System	PEC	3	0	0	3
5.	24ES212	Intelligent Control and Automation	PEC	3	0	0	3
6.	24ES213	Unmanned Aerial Vehicle	PEC	3	0	0	3
7.	24ES214	DSP Based System Design	PEC	3	0	0	3
8.	24ES215	Machine Learning and Deep Learning	PEC	3	0	0	3
9.	24ES302	Computer Vision	PEC	3	0	0	3
10.	24ES303	Multimedia Communication	PEC	3	0	0	3
11.	24ES304	Embedded Networking and Automation of Electrical System	PEC	3	0	0	3
12.	24ES305	Smart System Design	PEC	3	0	0	3
13.	24ES306	Embedded Computing	PEC	3	0	0	3
14.	24ES307	Embedded Systems Security	PEC	3	0	0	3
15.	24ES308	Robotics and Automation	PEC	3	0	0	3
16.	24ES310	Reconfigurable Processor and SoC Design	PEC	3	0	0	3
17.	24ES311	MEMS and NEMS Technology	PEC	3	0	0	3
18.	24ES312	Entrepreneurship and Embedded Product Development	PEC	3	0	0	3
19.	24ES313	Embedded System for Biomedical Applications	PEC	3	0	0	3
20.	24ES314	Renewable Energy and Grid Integration	PEC	3	0	0	3
21.	24ES315	Electric Vehicles and Power Management	PEC	3	1	0	4
22.	24ES316	Python Programming for Machine Learning	PEC	3	0	0	3
23.	24ES317	Smart Grid	PEC	3	0	0	3
Research Methodology Courses (RMC)							

S.No	Course Code	Course Title	Course Type	L	T	P	Credit
1.	24RM101	Research Methodology and IPR	RMC	2	0	0	2
Open Electives Courses (OEC)							
S.No	Course Code	Course Title	Course Type	L	T	P	Credit
1.	24CI341	Integrated Water Resources Management	OEC	3	0	0	3
2.	24CI342	Water, Sanitation and Health	OEC	3	0	0	3
3.	24CI343	Principles of Sustainable Development	OEC	3	0	0	3
4.	24CI344	Environmental Impact Assessment	OEC	3	0	0	3
5.	24CP311	Block chain Technologies	OEC	3	0	0	3
6.	24CP310	Deep Learning	OEC	3	0	0	3
7.	24IS342	Vibration and Noise Control Strategies	OEC	3	0	0	3
8.	24TE341	Energy Conservation and Management in Domestic Sectors	OEC	3	0	0	3
9.		Additive Manufacturing	OEC	3	0	0	3
10.	24TE342	Electric Vehicle Technology	OEC	3	0	0	3
11.	24TE343	New Product Development	OEC	3	0	0	3
12.	24CI345	Sustainable Management	OEC	3	0	0	3
13.	24IS341	Micro and Small Business Management	OEC	3	0	0	3
14.	24IS343	Intellectual Property Rights	OEC	3	0	0	3
15.	24IS344	Ethical Management	OEC	3	0	0	3
16.	24CP342	Security Practices	OEC	3	0	0	3
17.	24CP343	Cloud Computing Technologies	OEC	3	0	0	3
18.	24TC344	Design Thinking	OEC	3	0	0	3
19.	24CP341	Principles of Multimedia	OEC	3	0	0	3
20.	24CP345	Big Data Analytics	OEC	3	0	0	3
21.	24CP346	Internet of Things and Cloud	OEC	3	0	0	3
22.	24CP347	Medical Robotics	OEC	3	0	0	3
23.	24CP348	Embedded Automation	OEC	3	0	0	3
24.	24TE346	Environmental Sustainability	OEC	3	0	0	3
25.	24TE345	Textile Reinforced Composites	OEC	3	0	0	3
26.	24TE346	Nano composite Materials	OEC	3	0	0	3
27.	24RM342	IPR, Bio safety and Entrepreneurship	OEC	3	0	0	3
Employability Enhancement Courses (EEC)							
S.No	Course Code	Course Title	Course Type	L	T	P	Credit

1.	24ES251	Project Work - I	EEC	0	0	12	6
2.	24ES451	Project Work - II	EEC	0	0	24	12
Non Credit/ Audit Course							
S.No	Course Code	Course Title	Course Type	L	T	P	Credit
1.	24AC101	English for Research Paper Writing	AC	2	0	0	0
2.	24AC102	Disaster Management	AC	2	0	0	0
3.	24AC104	Constitution of India	AC	2	0	0	0



Recommended Courses for SEMESTER-I

S.No.	Course Code	Course Title	Category	L	T	P	C
THEORY COURSES							
1	24ES101	Applied Mathematics for Embedded Systems Technologists	FC	3	1	0	4
2	24RM101	Research Methodology and IPR	RMC	2	0	0	2
3	24ES102	Design of Embedded Systems	PCC	3	0	0	3
4	24ES103	Embedded System Networks	PCC	3	0	0	3
5	24ES104	Microcontroller Based System Design	PCC	3	0	0	3
6	24ES105	VLSI Design and Reconfigurable Architecture	PCC	3	0	0	3
7	24AC1XX	Audit Course I*	AC	2	0	0	0
LABORATORY COURSES							
8	24ES131	Embedded System Laboratory - I	PCC	0	0	4	2
9	24ES132	Programming and Algorithms Laboratory	PCC	0	0	4	2
TOTAL				19	1	8	22

Recommended Courses for SEMESTER-II

S.No.	Course Code	Course Title	Category	L	T	P	C
THEORY COURSES							
1	24ES201	Real Time Operating System	PCC	3	0	0	3
2	24ES202	Advanced Digital System Design	PCC	3	0	0	3
3	24ES203	Embedded Control for Electric Drives	PCC	3	0	0	3
4	24ES204	IoT for Smart Systems	PCC	3	0	0	3
5	24ES2XX	Professional Elective I	PEC	3	0	0	3
6	24ES2XX	Professional Elective II	PEC	3	0	0	3
7	24AC1XX	Audit Course II*	AC	2	0	0	0
LABORATORY COURSES							
8	24ES251	Embedded System Laboratory - II	PCC	0	0	4	2
9	24ES252	Embedded Programming Laboratory	PCC	0	0	4	2
TOTAL				20	0	8	22

Course Code:	24ES101	Course Title:	Applied Mathematics for Embedded Systems Technologists
Credits:	4	L – T – P	3 – 1 – 0

Course objectives:

- To understand the techniques of Fourier transform to solve partial differential equations.
- To become familiar with graph theory for modelling the embedded system.
- To acquire knowledge in probability, random variables and standard distributions
- To understand the basic concept of random variables and queuing theories to address stochastic and dynamic environment in embedded technology.

Teaching-Learning Process:

These are sample strategies which teachers can use to accelerate the attainment of the various course outcomes.

- Lecture method does not mean only traditional method, but different type of teaching methods may be adopted to develop the outcomes.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world and when that's possible, it helps to improve the students' understanding.

UNIT I –Fourier Transform Techniques for Partial Differential Equations**[12 hours]**

Fourier transform: Definitions - Properties – Transform of elementary functions - Dirac delta function – Convolution theorem – Parseval's identity – Solutions to partial differential equations: Heat equation - Wave equation - Laplace and Poisson's equations.

UNIT II – Graph Theory**[12 hours]**

Introduction to paths, trees, vector spaces - Matrix coloring and directed graphs - Some basic algorithms – Shortest path algorithms – Depth - First search on a graph – Isomorphism – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III – Optimization Techniques**[12 hours]**

Linear programming - Basic concepts – Graphical and simplex methods – Big M method - Two phase

simplex method - Revised simplex method - Transportation problems – Assignment problems.

UNIT IV – Probability and Random Variables	[12 hours]
Probability – Axioms of probability – Conditional probability – Baye’s theorem - Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Exponential, Normal distributions – Functions of one dimensional random variable.	

UNIT V – Queuing Theory	[12 hours]
Single and multiple servers - Markovian queuing models - Finite and infinite capacity queues – Finite source model – Queuing applications.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Use the mathematical principles on transforms and partial differential equations would provide them the ability to formulate and solve some of the physical problems of engineering
CO2	Apply Graph theory concept to solve real world application like routing, TSP/Traffic Control etc...
CO3	Construct a linear programming model from problem description, and apply the simple method for solving linear programming problems.
CO4	Apply the ideas of probability and random variables in solving engineering problems.
CO5	Apply the concept of Queuing Models in real life problems

COs and POs Mapping:

CO'S	PO1	PO2	PO3
CO1	2	3	1
CO2	3	3	2
CO3	3	3	2
CO4	2	2	1
CO5	3	3	1

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40

	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

Skill Assessment Components: Individual Assignment / Worksheet / Case Study / Mini Project

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. Taha H.A., " Operations Research: An Introduction “, 9th Edition, Pearson Education Asia, New Delhi, 2016.
2. Walpole R.E., Myer R.H., Myer S.L., and Ye, K., " Probability and Statistics for Engineers and Scientists ", 7th Edition, Pearson Education, Delhi, 2002.
3. Sankara Rao, K., “Introduction to Partial Differential Equations”, Prentice Hall of India Pvt. Ltd., New Delhi, 1997.
4. Narasingh Deo, " Graph Theory with Applications to Engineering and Computer Science ", Prentice Hall India, 1997.

Web Links and Video Lectures (E-Resources):

1. Probability Distributions: <https://www.nptelvideos.com/lecture.php?id=14400>
2. Applications of Fourier Transform to PDEs: <https://www.nptelvideos.com/lecture.php?id=13442>
3. Graph Theory: <https://www.nptelvideos.com/lecture.php?id=13728>

Equivalent NPTEL/SWAYAM Courses:

S.No.	Course Title	Course Instructor	Host Institute
1	Probability and Statistics	Prof. Somesh Kumar	IIT Kharagpur
2	Advanced Engineering Mathematics	Dr. P. Panigrahi Prof. J. Kumar Prof. P.D. Srivastava Prof. Somesh Kumar	IIT Kharagpur

Course Code:	24RM101	Course Title:	Research Methodology and IPR
Credits:	2	L – T – P	2-0-0

Course objectives:

To impart knowledge on the

- Importance of research methodology and Intellectual Property Rights.
- Rights for the protection of their invention done in their project work.
- Registration of patents in our country and foreign countries of invention, designs and thesis or theory written.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. NPTEL and Other Videos
5. Smart Class Room
6. Flipped Class

UNIT I –Research Design**[9 hours]**

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II – Data Collection and Sources**[9 hours]**

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods.
Data - Preparing, Exploring, examining and displaying.

UNIT III – Data Analysis and Reporting**[9 hours]**

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT IV – Intellectual Property Rights	[9 hours]
<p>Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.</p>	

UNIT V – Patents	[9 hours]
<p>Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filing, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.</p>	

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Formulate a research problem and explain the concepts related to research design
CO2	Depict the methods of data collection and analysis
CO3	Analyze research data and related information.
CO4	Understand the importance of IPR in growth of individuals & Nation.
CO5	Recognize the importance of Report writing.

COs and POs Mapping:

COs	PO1	PO2	PO3
CO1	2	1	1
CO2	2	1	-
CO3	2	1	1
CO4	2	2	-
CO5	2	3	-

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final mark

					ks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. D P Neeraj Pandey and Khushdeep Dharni, 'Intellectual Property Rights', First edition, PHI learning Pvt. Ltd., Delhi, 2014.
2. Uma Sekaran and Roger Bougie, 'Research methods for Business', 5th Edition, Wiley India, New Delhi, 2012.
3. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students", 2nd edition, Juta Academic, 2001.
4. Ramakrishna B & Anilkumar H S, 'Fundamentals of Intellectual Property Rights', 1st edition, Notion Press, 2017.

Reference Books:

1. William G Zikmund, Barry J Babin, Jon C. Carr, Atanu Adhikari, Mitch Griffin, "Business Research methods", A South Asian Perspective, 8th Edition, Cengage Learning, New Delhi, 2012.

Web Links and Video Lectures (E-Resources):

1. Research Methodology: https://onlinecourses.nptel.ac.in/noc23_ge36/preview
2. Intellectual Property: https://onlinecourses.nptel.ac.in/noc22_hs59/preview

Suggested Skill Activities:

1. Case Study Analysis:

- Select a research paper or real-world case study related to a specific research methodology (qualitative, quantitative, mixed methods, etc.).
- Critically analyze the methodology used, its strengths, weaknesses, and appropriateness for the research question.
- Discuss alternative methodologies that could have been used and their implications.

2. Designing Research Proposals:

- Divide students into groups and assign them different research topics.
- Have each group develop a research proposal including research questions, objectives, methodology, sampling techniques, and data analysis methods.
- Present proposals to the class for peer review and feedback.

3. Data Analysis Exercises:

- Provide students with datasets (real or simulated) and ask them to perform various types of data analysis (descriptive statistics, regression analysis, content analysis, etc.).
- Emphasize interpretation of results and drawing meaningful conclusions based on data.

4. IPR Case Analysis:

- Assign students to analyze landmark intellectual property cases.
- Discuss the legal principles involved (e.g., infringement, fair use, licensing agreements) and the impact of these cases on IPR law.

5. Trademark and Copyright Exercises:

- Ask students to identify trademarks and copyrights in everyday products or creative works.
- Discuss the process of registering trademarks and copyrights, and the benefits of intellectual property protection for businesses and creators.

Course Code:	24ES102	Course Title:	Design of Embedded systems
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To provide knowledge on the basics, building blocks of Embedded System.
- To discuss Input/output Interfacing & Bus Communication with processors.
- To Teach automation using scheduling algorithms and Real time operating system.
- To Identify the design approaches for uniprocessor and multiprocessor
- To Interpret on different Phases & Modeling of a new embedded product.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Power point presentation
3. Blended Mode of Learning
4. Project based Learning
5. Experiential Learning
6. NPTEL and Other Videos
7. Smart Class Room
8. Flipped Class

UNIT I – INTRODUCTION TO EMBEDDED SYSTEMS**[9
hours]**

Introduction to Embedded Systems –built in features for embedded Target Architecture - selection of Embedded processor – DMA- memory devices – Memory management methods-memory mapping - cache replacement policies- Timer and Counting devices- Watchdog Timer - Real Time Clock - Software Development tools-IDE - assembler – compiler – linker – simulator – debugger

UNIT II – EMBEDDED NETWORKING BY PROCESSORS**[9
hours]**

Embedded Networking: Introduction - I/O Device Ports & Buses- multiple interrupts and interrupt service mechanism – Serial Bus communication protocols -RS232 standard–RS485–USB–Inter Integrated Circuits (I2C)- CAN Bus –Wireless protocol based on Wifi– Bluetooth - Zigbee

UNIT III – RTOS BASED EMBEDDED SYSTEM DESIGN**[9
hours]**

Introduction to basic concepts of RTOS- Need, Task, process & threads- interrupt routines in RTOS- Multiprocessing and Multitasking - Preemptive and non-preemptive scheduling - Task communication context switching- interrupt latency and deadline shared memory- message passing- Interprocess Communication – synchronization between processes-semaphores, Mailbox- pipes- priority inversion, priority inheritance- comparison of Real time-Operating systems – VxWorks- uC/OS-II, RT Linux

UNIT IV – MODELLING WITH HARDWARE/SOFTWARE DESIGN APPROACHES**[9
hours]**

Modelling embedded systems- embedded software development approach --Overview of UML modeling with UML, UML Diagrams-- Hardware/Software Partitioning- Co-Design Approaches for System Specification and modeling- CoSynthesis- features comparing -Single-processor Architectures

& Multi-Processor Architectures--design approach on parallelism in uniprocessors & Multiprocessors.

UNIT V – EMBEDDED SYSTEM APPLICATION DEVELOPMENT

**[9
hours]**

Objectives, different Phases & Modeling of the Embedded product development life cycle (ELDC). - Case studies on Digital Camera, Adaptive Cruise control in a Car, Mobile Phone software for key inputs.

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Demonstrate the functionalities of processor internal blocks, based on their requirement.
CO2	Analyze the Bus standards are chosen based on interface overheads to improve processor performance
CO3	Analyze the role and features of RT operating system, that makes multitask execution possible by processors.
CO4	Apply multiple CPU based on either hardcore or softcore helps data overhead management with processing- speed reduction for processor execution.
CO5	Apply Embedded consumer product design based on phases of product development.

COs and POs Mapping:

CO's	PO1	PO2	PO3
CO1	2	2	-
CO2	3	2	-
CO3	3	2	-
CO4	2	1	-
CO5	2	1	-

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		

	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. Rajkamal, 'Embedded system-Architecture, Programming, Design', TMH,2011.
2. Peckol, "Embedded system Design",JohnWiley&Sons,2010

Reference Books:

1. Lyla B Das," Embedded Systems-An Integrated Approach",Pearson2013
2. Elicia White," Making Embedded Systems", O'Reilly Series,SPD,2011
3. Bruce Powel Douglass," Real-Time UML Workshop for Embedded Systems,Elsevier,2011
4. Advanced Computer architecture , By Rajiv Chopra, S Chand , 2010
5. Jorgen Staunstrup, Wayne Wolf ,Hardware / Software Co- Design Principles and Practice, Springer, 2009.

Web Links and Video Lectures (E-Resources):

1. Embedded system design: <https://archive.nptel.ac.in/courses/108/102/108102169/>

Suggested Skill Activities:

1. Design and Implement a Processor:
 - Task students with designing a simple processor architecture (such as a reduced instruction set computer, RISC) using FPGA tools like Verilog or VHDL.
 - Include components like instruction decoding, ALU operations, and memory access.
2. Real-World Applications and Projects:
 - Assign projects related to real-world signal processing applications, such as audio processing, video compression, or wireless communication systems.

Course Code:	24ES103	Course Title:	Embedded System Networking
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To expose the students to the fundamentals of wired embedded networking techniques.
- To introduce the concepts of embedded ethernet.
- To expose the students to the fundamentals of wireless embedded networking.
- To discuss the fundamental building blocks of digital instrumentation.
- To introduce design of Programmable measurement & control of electrical Device

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. PowerPoint presentation
3. Interactive Simulations
4. Lab experiment videos
5. Blended Mode of Learning
6. Project based Learning
7. Experiential Learning
8. NPTEL and Other Videos
9. Smart Class Room
10. Flipped Class

UNIT I - EMBEDDED PROCESS COMMUNICATION WITH INSTRUMENT BUS	[9 hours]
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Embedded networking: Introduction – Cluster of instruments in System: Introduction to bus protocols – comparison of bus protocols – RS 232C, RS 422, RS 485 and USB standards – embedded ethernet – MOD bus, LIN bus and CAN bus.

UNIT II – EMBEDDED ETHERNET	[9 hours]
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Elements of a network – Inside Ethernet – Building a Network : Hardware options – Cables, Connections and network speed – Ethernet controllers – Inside the internet protocol – Exchanging messages using UDP and TCP – Email for Embedded systems using FTP – Keeping devices and network secure

UNIT III – WIRELESS EMBEDDED NETWORKING	[9 hours]
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Wireless sensor networks – Introduction – Node architecture – Network topology -Localization – Time synchronization – Energy efficient MAC protocols – SMAC – Energy efficient and robust

routing – Data centric routing - WSN Applications - Home Control - Building Automation - Industrial Automation

UNIT IV – BUILDING SYSTEM AUTOMATION

**[9
hours]**

Sensor Types & Characteristics: Sensing Voltage, Current, flux, Torque, Position, Proximity, Accelerometer - Data acquisition system- Signal conditioning circuit design- Uc Based & PC based data acquisition – UC for automation and protection of electrical appliances –processor based digital controllers for switching Actuators: Stepper motors, Relays –System automation with multi-channel Instrumentation and interface

**UNIT V –COMMUNICATION FOR LARGE ELECTRICAL SYSTEM
AUTOMATION**

**[9
hours]**

Data Acquisition, Monitoring, Communication, Event Processing, and Polling Principles, SCADA system principles – outage management– Decision support application - substation automation, extended control feeder automation, Performance measure and response time, SCADA Data Models, need, sources, interface

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Analyze the different bus communication protocols used for embedded networking
CO2	Explain the basic concepts of embedded networking
CO3	Apply the embedded networking concepts in wireless networks
CO4	Relate different data acquisition concepts.
CO5	Build a system automation for different applications

COs and POs Mapping:

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	-	-	3	1
CO2	-	2	-	-	2	1
CO3	3	2	2	3	2	3
CO4	2	-	3	3	-	2
CO5	3	-	3	3	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	25
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	35	50	50
	Lab Exam	100	15		
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.
 1. **Text Books:** Mohammad Ilyas And Imad Mahgoub, 'Handbook of sensor Networks: Compact wireless and wired sensing systems', CRC Press, 2005.

Reference Books:

1. Krzysztof Iniewski, "Smart Grid ,Infrastructure & Networking", TMcGH, 2012.

Course Code:	24ES104	Course Title:	Microcontroller Based System Design
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To illustrate the architecture of PIC Microcontroller and RISC processor.
- To compare the architecture and programming of 8,16,32 bit RISC processor.
- To construct the implementation of DSP in ARM processor.
- To discuss on memory management, application development in RISC processor.
- To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Interactive Simulations
3. Lab experiment videos
4. Blended Mode of Learning
5. Project based Learning
6. Experiential Learning
7. NPTEL and Other Videos
8. Smart Class Room
9. Flipped Class

UNIT I – PIC Microcontroller**[9
hours]**

Architecture - memory organization - addressing modes - instruction set - PIC programming in Assembly & C - I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, practice in MP-LAB.

UNIT II – ARM Architecture**[9
hours]**

Architecture - memory organization - addressing modes - The ARM Programmer's model - Registers - Pipeline - Interrupts - Coprocessors – Interrupt Structure

UNIT III – Peripherals of PIC and ARM Microcontroller**[9
hours]**

PIC: ADC, DAC and Sensor Interfacing –Flash and EEPROM memories. ARM: I/O Memory – EEPROM – I/O Ports – SRAM –Timer –UART - Serial Communication with PC – ADC/DAC Interfacing.

UNIT IV – ARM Microcontroller Programming**[9
hours]**

ARM general Instruction set – Thumb instruction set –Introduction to DSP on ARM – Implementation example of Filters

UNIT V –Design with PIC And ARM Microcontrollers**[9
hours]**

PIC implementation - Generation of Gate signals for converters and Inverters - Motor Control – Controlling DC/ AC appliances – Measurement of frequency - Standalone Data Acquisition System –ARM Implementation- Simple ASM/C programs- Loops –Look up table- Block copy-

subroutines-Hamming Code.

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Illustrate the basics and requirement of processor functional blocks.
CO2	Demonstrate the specialty of RISC processor Architecture.
CO3	Make use of I/O hardware interface of a processor based automation for consumer application with peripherals.
CO4	Construct I/O software interface of a processor with peripherals.
CO5	Utilize PIC and Arm Microcontrollers for Controlling DC/ AC appliances

COs and POs Mapping:

COs	PO1	PO2	PO3
CO1	-	-	2
CO2	1	-	3
CO3	-	-	1
CO4	-	-	-
CO5	1	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Theory Exam	100	65	60	60

	Total	100
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End semester Examination: (OP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. Steve Furber, ‘ARM system on chip architecture’, Addison Wesley, 2010.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield ‘ARM System Developer’s Guide Designing and Optimizing System Software’, Elsevier 2007.
3. Muhammad Ali Mazidi, Rolin D. McKinlay, Danny Causey ‘PIC Microcontroller and Embedded Systems using Assembly and C for PIC18’, Pearson Education 2008.

Reference Books:

1. John Iovine, ‘PIC Microcontroller Project Book’, McGraw Hill 2000
2. William Hohl, ‘ARM Assembly Language’ Fundamentals and Techniques, 2009.
3. Rajkamal, ‘Microcontrollers Architecture, Programming, Interfacing, & System Design’, Pearson, 2012
4. ARM Architecture Reference Manual, LPC213x User Manual

Web Links and Video Lectures (E-Resources):

1. Advanced ARM Cortex Processors: www.Nuvoton.com

Suggested Skill Activities:

1. Real-World Applications and Case Studies:
 - Assign projects that involve designing embedded systems using PIC/ARM for specific applications (e.g., robotics control, industrial automation).

Course Code:	24ES105	Course Title:	VLSI Design and Reconfigurable Architecture
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- Sequential system design, synchronous and Asynchronous circuits.
- Basic concepts of CMOS and to introduce the IC fabrication methods
- Reconfigurable Processor technologies and to provide an insight and architecture significance of SOC in real time application.
- Basics of analog VLSI design and its importance.

- Programming of Programmable device using Hardware description Language.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I –Introduction to Advanced Digital System Design

[9
hours]

Modeling of Clocked Synchronous Sequential Network (CSSN), Design of CSSN, Design of Asynchronous Sequential Circuits (ASC), Designing Vending Machine Controller, Races in ASC, Static and Dynamic Hazards, Essential Hazards, Designing Hazard free circuits

UNIT II – CMOS Basics & IC Fabrication

[9
hours]

Moore's Law-MOSFET Scaling - MOS Transistor Model-Determination of pull up / pull down ratios CMOS based combinational logic & sequential design- Dynamic CMOS –Transmission Gates-BiCMOS- Low power VLSI – CMOS IC Fabrications - Stick Diagrams, Design Rules and Layout.

UNIT III – ASIC and Reconfigurable Processor and SoC Design

[9
hours]

Introduction to ASIC, ASIC design flow- programmable ASICs- Introduction to reconfigurable processor- Architecture -Reconfigurable Computing, SoC Overview, recent trends in Reconfigurable Processor & SoC, Reconfigurable processor based DC motor control.

UNIT IV – Analog VLSI Design	[9 hours]
Introduction to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp –High Speed and High frequency op-amps-Super MOS- Analog primitive cells- Introduction to FPAA.	

UNIT V – VHDL Programming	[9 hours]
Overview of digital design with VHDL, structural, data flow and behavioural modeling concepts- logic synthesis-simulation-Design examples, Ripple carry Adders, Carry Look ahead adders, Multiplier, ALU, Shift Registers, Test Bench.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Incorporate synchronous and asynchronous switching logics, with clocked circuits design
CO2	Deliver insight into developing CMOS design techniques and IC fabrication methods.
CO3	Explain the need of reconfigurable computing, hardware-software design and operation of SoC processor.
CO4	Design and development of reprogrammable analog devices and its usage for Embedded applications.
CO5	Illustrate and develop HDL computational processes with improved design strategies.

COs and POs Mapping:

CO'S	PO1	PO2	PO3
CO1	-	-	-
CO2	2	-	2
CO3	-	-	3
CO4	2	-	2
CO5	-	1	1

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Mark	Reduced	Total	Final marks

		s	Marks		
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
2. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.
3. Nurmi, Jari (Ed.) "Processor Design System-On-Chip Computing for ASICs and FPGAs" Springer, 2007.
4. Joao Cardoso, Michael Hübner, "Reconfigurable Computing: From FPGAs to Hardware/Software Codesign" Springer, 2011.
5. Pierre-Emmanuel Gaillardon, Reconfigurable Logic: Architecture, Tools, and Applications, 1st Edition, CRC Press , 2015
6. Mohamed Ismail ,TerriFiez, “Analog VLSI Signal and information Processing”, McGraw Hill International Editions,1994.
7. William J. Dally / Curtis Harting / Tor M. Aamodt,” Digital Design Using VHDL:A Systems Approach, Cambridge Univerity Press,2015.
8. ZainalatsedinNavabi, ‘VHDL Analysis and Modelling of Digital Systems’, 2n Edition, Tata McGraw Hill, 1998.

Suggested Skill Activities:

1. Develop a reconfigurable computing, hardware-software design and operation of SoC processor.

Course Code:	24ES131	Course Title:	Embedded System Laboratory – I
Credits:	2	L – T – P	0-0-4

Course objectives:

To impart knowledge on the

- To involve the students to Practice on Workbench /Software Tools/ Hardware Processor Boards with the supporting Peripherals.
- To teach the concepts of algorithm development & programming on software tools and Digital processors with peripheral interfaces.
- To encourage students to practice in open source software/packages/tools
- To train through hands-on practices in commercial and licensed Hardware-software suites
- Practicing through the subdivisions covered within experiments listed below to expose the students into the revising the concepts acquired from theory subjects.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. NPTEL and Other Videos
3. Smart Classroom
4. Flipped Class

Laboratory Component

[60 hours]

S.No.	Name of the Experiment
1	Programming with 8 bit Microcontrollers # Assembly programming
2	Programming with 8 bit Microcontrollers # C programming
3	I/O Programming with 8bit Microcontrollers I/O Interfacing :Serial port programming/LCD/Sensor Interfacing /PWM Generation/Motor Control
4	Programming with PIC Microcontrollers: Assembly Cprogramming
5	I/O Programming with PIC Microcontrollers I/O Interfacing : PWM Generation/ Motor Control/ADC/DAC/ LCD/Sensor Interfacing

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Experiment with the embedded processors of CISC and RISC architecture/ computational processors with peripheral interface.
CO2	Analyze the microcontroller-based process control with the conventional control impact.
CO3	Experiment with the programming logic of Processor based on software suites (simulators, emulators)
CO4	Apply I/O software interface of a processor with peripherals for transferring information/data.
CO5	Analyze the influence of recent interfacing trends and use of commercial embedded processors.

COs and POs Mapping:

CO'S	PO1	PO2	PO3
CO1	2	1	2
CO2	-	-	1
CO3	2	3	1
CO4	2	-	2
CO5	-	-	1
CO	2	2	1.4

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Laboratory	Continuous Assessment	75	75	100	60
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Lab Exam	100	40	40	40
				Total	100

End semester Examination: (OP PATTERN)

- Each unit consists of two 2 marks questions and one 13 marks question (either or).
- One 16 marks question (either or) will be from any one of the five units.
- All the sixteen questions have to be answered.

REFERENCE BOOKS

1. Mohammad Ali Mazidi & Mazidi '8051 Microcontroller and Embedded Systems', Pearson Education

2. Mohammad Ali Mazidi, Rolind Mckinley and Danny Causey, 'PIC Microcontroller and Embedded

Systems' Pearson Education.

3. Simon Monk, "Make Action-with Arduino and Raspberry Pi,SPD,2016.
4. Wesley J.Chun, "Core Python Applications Programming,3rded,Pearson,2016
5. Kraig Mitzner, 'Complete PCB Design using ORCAD Capture and Layout', Elsevier
6. Vinay K.Ingle, John G.Proakis,"DSP-A Matlab Based Approach", Cengage Learning, 2010.
7. Taan S.Elali, "Discrete Systems and Digital Signal Processing with Matlab", CRC Press 2009.
8. Jovitha Jerome, "Virtual Instrumentation using Lab view" PHI, 2010.
9. Woon-Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture', John Wiley & Sons, Inc., Hoboken, New Jersey 2007
10. Dogan Ibrahim, 'Advanced PIC microcontroller projects in C',Elsevier2008
11. Perry Lea, "Internet of things for architects," Packt, 2018.

Skill Assessment:

1. Do a project to control traffic light using PIC microcontroller.
2. Write an detailed report on comparison between PIC Microcontroller and 8 bit microcontroller.

Course Code:	24ES132	Course Title:	PROGRAMMING AND ALGORITHMS LABORATORY
Credits:	2	L – T – P	0-0-4

Course objectives:

- To develop an algorithm & programming on software tools and Digital processors with peripheral interfaces.
- To expertise in open source software / packages /tools.
- To do hands-on in commercial and licensed Hardware-software suites.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Interactive Simulations
2. Lab experiment videos
3. Blended Mode of Learning
4. Project based Learning
5. Experiential Learning
6. NPTEL and Other Videos
7. Smart Class Room
8. Flipped Class

LIST OF EXPERIMENTS

1. Implementation of basic programming concepts like conditionals and loops
2. Implementation of function and operator overloading
3. Creation of classes and objects.
4. Implementation of constructors and destructors
5. Implementation of array of objects and dynamic objects.
6. Implementation of inheritance and its types
7. Implementation of polymorphism and its types.
8. Implementation of various sorting algorithms.
9. Application of Stack
10. Implementation of queue using array.
11. Implementation of Linked Lists: Singly linked, doubly linked and Circular lists and applications.

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Implement various object oriented concepts through simple programs.
CO2	Implement different data structures using C++
CO3	Apply the different data structures for implementing solutions to practical problems
CO4	Demonstrate searching algorithms
CO5	Demonstrate sorting algorithms

COs and POs Mapping:

CO/PO	PO1	PO2	PO3
CO1	3	-	2
CO2	3	-	2
CO3	3	-	2
CO4	3	-	2
CO5	3	-	2
CO	3	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Laboratory	Continuous Assessment	75	75	100	60
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Lab Exam	100	40	40	40
				Total	100

Course Code:	24ES201	Course Title:	Real Time Operating System
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To explore the fundamental interaction of OS with a computer and User computation.
- To explain the fundamental concepts of how process are created and controlled with OS.
- To study on programming logic of modeling Process based on range of OS features
- To compare types and Functionalities in commercial OS, application development using RTOS
- To develop real time application with RTOS.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Interactive Simulations
3. Lab experiment videos
4. Blended Mode of Learning
5. Project based Learning
6. Experiential Learning
7. NPTEL and Other Videos
8. Smart Class Room
9. Flipped Class

UNIT I – Review of Operating Systems	[9 hours]
Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Introduction to Distributed operating system – Embedded operating systems	
UNIT II – Overview of RTOS	[9 hours]
RTOS Task and Task state –Multithreaded Preemptive scheduler- Process Synchronization- Message queues– Mail boxes -pipes – Critical section – Semaphores – Classical synchronization problem – Deadlocks	
UNIT III – Realtime Models and Languages	[9 hours]
Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.	
UNIT IV – Realtime Kernel	[9 hours]
Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and Basic study of various RTOS like – VX works – Linux supportive RTOS – C Executive.	
UNIT V –Application Development	[9 hours]
Discussions on Basics of Linux supportive RTOS – uCOS-C Executive for development of RTOS Application – Case study	

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Outline Operating System structures and types
CO2	Insight into scheduling, disciplining of various processes execution.
CO3	Illustrate knowledge on various RTOS support modelling
CO4	Demonstrate commercial RTOS Suite features to work on real time processes design.
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in RTOS and embedded automation design.

COs and POs Mapping:

COs	PO1	PO2	PO3
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CO1	2	2	2
CO2	2	3	2
CO3	1	2	1
CO4	2	3	2
CO5	2	3	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Theory Exam	100	65	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in RTOS and embedded automation design.

Reference Books:

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.

Web Links and Video Lectures (E-Resources):

1. Real Time Operating System: <https://archive.nptel.ac.in/courses/106/105/106105172/>

Suggested Skill Activities:

1. RTOS Task Creation and Management:
 - Task students with creating tasks in an RTOS environment (e.g., FreeRTOS, VxWorks).
 - Assign different priorities to tasks and observe how the RTOS scheduler manages task execution based on priority levels.

- Discuss the concepts of preemption, context switching, and task scheduling algorithms (e.g., priority scheduling, round-robin).

2. Real-World Applications and Case Studies:

- Assign projects that involve designing embedded systems using RTOS for specific applications (e.g., robotics control, industrial automation).
- Encourage students to integrate sensor inputs, actuator controls, and communication interfaces within an RTOS framework.

Course Code:	24ES202	Course Title:	Advanced Digital System Design
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To infer the modelling of clocked synchronous sequential networks.
- To interpret and design the asynchronous sequential circuit in various modes.
- To diagnose the faults and test the system using defined algorithms.
- To identify the need of EPROM technology to realize the sequential circuits.
- To utilize the VHDL principle for describing the combinational circuits.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Lab experiment videos
3. Blended Mode of Learning
4. Project based Learning
5. Experiential Learning
6. NPTEL and Other Videos
7. Smart Class Room
8. Flipped Class

UNIT I – Sequential Circuit Design	[9 hours]
Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.	

UNIT II – Asynchronous Sequential Circuit Design	[9 hours]
Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.	
UNIT III – Fault Diagnosis And Testability Algorithms	[9 hours]
Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.	
UNIT IV – Synchronous Design Using Programmable Devices	[9 hours]
EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000.	
UNIT V – System Design Using VHDL	[9 hours]
VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Apply the design procedure of clocked synchronous and asynchronous sequential circuits for developing simple digital system.
CO2	Analyze the clocked synchronous sequential circuits and asynchronous sequential circuits in digital system.
CO3	Interpret the basic and advanced concepts in testing the digital circuits for real world applications.
CO4	Apply the EPROM techniques to design synchronous sequential circuit using programmable devices.
CO5	Infer the basics of programming the VHDL for digital circuit design.

COs and POs Mapping:

CO's	PO1	PO2	PO3
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CO1	3	2	-
CO2	-	3	-
CO3	3	-	-
CO4	2	2	-
CO5	-	-	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. Donald G. Givone, “Digital principles and Design”, 1st Edition, Tata McGraw Hill, 2017.
2. Charles H. Roth Jr., “Digital System Design using VHDL”, 2nd Edition, Cengage Learning, 2007.

Reference Books:

1. Parag K Lala, “Digital System design using PLD” 1st Edition BS Publications, 2003.
2. Skahill. K, “VHDL for Programmable Logic” Pearson Education, 2010.
3. Robert K Dueck, “Digital Design with CPLD applications and VHDL”, Thomson Asia, 2004.

Web Links and Video Lectures (E-Resources):

1. Digital VLSI Testing: <https://archive.nptel.ac.in/courses/117/105/117105137/>
2. Digital electronic and System design: https://onlinecourses.nptel.ac.in/noc21_ee39/preview

Suggested Skill Activities:

1. Real-World Applications and Projects:
 - Assign projects related to real-world signal processing applications, such as audio processing, video compression, or wireless communication systems.
 2. Design Reviews and Presentations:
 - Organize design reviews where students present their projects to peers and instructors.
- Emphasize clear explanation of design choices, challenges faced, and solutions implemented.

Course Code:	24ES203	Course Title:	EMBEDDED CONTROL FOR ELECTRIC DRIVES
Credits:	3	L – T – P	3-0- 0

Course objectives:

To impart knowledge on the

- To provide the control concept for electrical drives
- To emphasize the need for embedded system for controlling the electrical drives
- To provide knowledge about various embedded system based control strategy for electrical drives
- To impart the knowledge of optimization and machine learning techniques used for electrical drives
- To familiarize the high performance computing for electrical drives.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Interactive Simulations
3. Lab experiment videos
4. Blended Mode of Learning
5. Project based Learning
6. Experiential Learning
7. NPTEL and Other Videos
8. Smart Class Room
9. Flipped Class

UNIT I – INTRODUCTION ELECTRICAL DRIVES	[9 hours]
Electric drive and its classifications, Four-quadrant drive, Dependence of load torque on various factors, Dynamic of motor-load combination- Solid State Controlled Drives- Machine learning and optimization techniques for electrical drives- IoT for Electrical drives applications.	
UNIT II – OVERVIEW OF EMBEDDED PROCESSOR	[9 hours]
Embedded Processor architecture-RTOS – Hardware/software co-design-Programming with SoC processors.	
UNIT III – INDUCTION MOTOR CONTROL	[9 hours]
Types- Speed control methods-PWM techniques- VSI fed three-phase induction motor- Fuzzy logic based speed control for three phase induction motor- FPGA based three phase induction motor control.	
UNIT IV – BLDC MOTOR CONTROL	[9 hours]
Overview of BLDC Motor -Speed control methods -PWM techniques- ARM processor based BLDC motor control-ANN for BLDC Motor control and operation.	
UNIT V – SRM MOTOR CONTROL	[9 hours]
Overview of SRM Motor -Speed control methods -PWM techniques- FPGA based SRM motor control-DNN for SRM Motor control and operation.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Interpret the significance of embedded control of electrical drives
CO2	Deliver insight into various control strategy for electrical drives
CO3	Developing knowledge on Machine learning and optimization techniques for motor control
CO4	Develop embedded systems solution for real time applications such as Electric vehicles and UAVs.
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systems skills required for motor control strategy

COs and POs Mapping:

COS	PO1	PO2	PO3
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CO1	1	-	2
CO2	1	1	3
CO3	2	-	-
CO4	1	2	3
CO5	-	-	-

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. R. Krishnan, "Electric Motor Drives—Modeling, Analysis and Control", Prentice-Hall of India Pvt. Ltd., New Delhi, 2010.
2. Vedam Subramanyam, "Electric Drives—Concepts and Applications", Tata McGraw-Hill publishing company Ltd., New Delhi, 2002

Reference Books:

1. K. Venkataratnam, Special Electrical Machines, Universities Press, 2014
2. Steve Furber, 'ARM system on chip architecture', Addison Wesley, 2010
3. Ron Sass and Andrew G. Schmidt, "Embedded System design with platform FPGAs: Principles and Practices", Elsevier, 2010.
4. Steve Kilts, "Advanced FPGA Design: Architecture, Implementation, and Optimization" Willey, 2007

Web Links and Video Lectures (E-Resources):

1. A Basic Course on Electric drive :https://onlinecourses.nptel.ac.in/noc24_ee125/preview
2. Basic Electrical drives: https://onlinecourses.nptel.ac.in/noc24_ee112/preview
3. Digital drive Circuits: https://onlinecourses.nptel.ac.in/noc24_ee147/preview

Suggested Skill Activities:

1. List the different speed control of machines, and prepare their rating chart.
2. Design the embedded based electrical drive.
3. Develop FPGA based three phase AC motor drive
4. Develop IOT based solutions for engineering applications.
5. Design ARM processor for BLDC motor control.

Course Code:	24ES204	Course Title:	IoT for Smart Systems
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- Internet of Things and its role in real time applications.
- Infrastructure required for IoT
- Communication techniques for IoT.
- Embedded processor and sensors required for IoT
- Different platforms and Attributes for IoT.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

10. Chalk and Talk
11. NPTEL and Other Videos
12. Smart Classroom
13. Flipped Class

UNIT I –I Introduction to Internet of Things	[9 hours]
Overview, Hardware and software requirements for IOT, Sensor and actuators, Technology drivers, Business drivers, Typical IoT applications, Trends and implications.	

UNIT II – IOT Architecture	[9 hours]
IoT reference model and architecture -Node Structure - Sensing, Processing, Communication, Powering, Networking - Topologies, Layer/Stack architecture, IoT standards, Cloud computing for IoT, Bluetooth, Bluetooth Low Energy beacons.	

UNIT III – Protocol and Wireless Technologies For IOT	[9 hours]
PROTOCOLS: NFC, SCADA and RFID, Zigbee MIPI, M-PHY, UniPro, SPMI, SPI, M-PCIE GSM, CDMA, LTE, GPRS, small cell. Wireless technologies for IoT: WiFi (IEEE 802.11), Bluetooth/ Bluetooth Smart, ZigBee/ZigBee Smart, UWB (IEEE 802.15.4), 6LoWPAN, Proprietary Systems-Recent trends.	

UNIT IV – IOT Processors	[9 hours]
Services/Attributes: Big-Data Analytics for IOT, Dependability, Interoperability, Security, Maintainability. Embedded processors for IOT: Introduction to Python programming -Building IOT with RASPBERRY PI and Arduino.	

UNIT V – Case Studies	[9 hours]
Industrial IoT, Home Automation, smart cities, Smart Grid, connected vehicles, electric vehicle charging, Environment, Agriculture, Productivity Applications, IOT Defense.	

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Explain the basic concepts and architecture of the Internet of Things.
CO2	Apply the IoT model to design basic IoT systems
CO3	Develop IoT applications using standards like MIPI, M-PHY, UniPro, SPMI, SPI, M-PCIE, and small cell technologies.
CO4	Develop IoT solutions using embedded processors such as Raspberry Pi and Arduino.
CO5	Implement IoT solutions for smart applications

COs and POs Mapping:

CO'S	1	2	3
CO1	2	1	-
CO2	3	2	1
CO3	3	2	1
CO4	3	2	1

CO5	3	2	1
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Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the sixteen questions have to be answered.

TEXT BOOKS

1. Robert Barton, Patrick Grossetete, David Hanes, Jerome Henry, Gonzalo Salgueiro, "IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things", CISCO Press, 2017
2. Samuel Greengard, The Internet of Things, The MIT Press, 2015

REFERENCE BOOKS

1. Arshdeep Bahga and VijaiMadiseti : A Hands-on Approach "Internet of Things", Universities Press 2015.
2. Oliver Hersent, David Boswarthick and Omar Elloumi "The Internet of Things", Wiley, 2016.
3. Adrian McEwen and Hakim Cassimally "Designing the Internet of Things" Wiley, 2014.
4. Ovidiu Vermesan and Peter Friess (Editors), "Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems", River Publishers Series in Communication, 2013.

WEB LINKS AND VIDEO LECTURES (E-RESOURCES):

1. Introduction and Definition of IOT: <https://youtu.be/IZOKa0Bh83o?si=9BJ023QXTEp8-26m>
2. Design of IOT: <https://youtu.be/urUBLmXFK10?si=mAcwX69fnPz0T0TG>
3. IOT Protocols: <https://youtu.be/TrFaCBV7joY?si=jl8jLARS57xxAmKb>
4. Case study- Healthcare: https://youtu.be/VeMDQHyBSaA?si=LfTyMi1PRH_1y28Q

5. Case Study: <https://youtu.be/6cklshRSUmk?si=b3KzmOLxJEbSCjTk>

Course Code:	24ES251	Course Title:	Embedded System Laboratory – II
Credits:	2	L – T – P	0-0-4

Course objectives:

To impart knowledge on the

- To involve the students to Practice on Workbench /Software Tools/ Hardware Processor Boards with the supporting Peripherals.
- To teach the concepts of algorithm development & programming on software tools and Digital processors with peripheral interfaces.
- To encourage students to practice in open source softwares/packages/tools
- To train through hands-on practices in commercial and licensed Hardware-software suites
- Practicing through the subdivisions covered with in experiments listed below to expose the students into the revising the concepts acquired from theory subjects.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. NPTEL and Other Videos
3. Smart Classroom
4. Flipped Class

Laboratory Component

[60 hours]

S.No.	Name of the Experiment
1	Programming ARM processor: ARM7 / ARM9/ARM Cortex Study on In-circuit Emulators, cross compilers, debuggers
2	I/O Programming with ARM processor: ARM7 / ARM9/ARM Cortex Microcontrollers I/O Interfacing: Timers/Interrupts/Serial port programming/PWM Generation/ Motor Control/ADC/DAC/ LCD/ RTC Interfacing/ Sensor Interfacing
3	Programming with Raspberry Pi Microcontroller Board: Study on incircuit Emulators, cross compilers, debuggers
4	I/O Programming with Arduino ,Raspberry Pi Microcontroller Boards I/O Interfacing: Timers/ Interrupts/ Serial port programming/PWM Generation/ Motor Control/ADC/DAC/ LCD/ RTC Interfacing/ Sensor Interfacing/IoT Applications
5	Programming with DSP processors
6	Study of one type of Real Time Operating Systems (RTOS)

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Experiment and demonstrate with simulators, in programming processor boards , processor interfacing/ designing digital controllers
CO2	Design & simulate Arithmetic ,Logic programs, Filters, Signal analysis with simulators/experiments ,in programming processor boards, processor interfacing/ Tools.
CO3	Develop real time solution for embedded applications.
CO4	Analyze Program and compile in various tools &soft ware domains.
CO5	Analyze the influence of recent interfacing trends and use of commercial embedded processors.

COs and POs Mapping:

CO'S	1	2	3
CO1	1	3	1
CO2	-	1	2
CO3	1	-	3
CO4	2	2	3
CO5	3	2	3
CO	1.75	2	2.4

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Laboratory	Continuous Assessment	75	75	100	60
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Lab Exam	100	40	40	40
				Total	100

End semester Examination: (OP PATTERN)

- Each unit consists of two 2 marks questions and one 13 marks question (either or).
- One 16 marks question (either or) will be from any one of the five units.
- All the sixteen questions have to be answered.

REFERENCE BOOKS

1. Mohamammad Ali Mazidi & Mazidi '8051 Microcontroller and Embedded Systems', Pearson Education
2. Mohammad Ali Mazidi, Rolind Mckinley and Danny Causey, 'PIC Microcontroller and Embedded Systems' Pearson Education
3. Simon Monk, "Make Action-with Arduino and Raspberry Pi, SPD, 2016.
4. Wesley J. Chun, "Core Python Applications Programming, 3rd ed, Pearson, 2016
5. Kraig Mitzner, 'Complete PCB Design using ORCAD Capture and Layout', Elsevier
6. Vinay K. Ingle, John G. Proakis, "DSP-A Matlab Based Approach", Cengage Learning, 2010.
7. Taan S. Elali, "Discrete Systems and Digital Signal Processing with Matlab", CRC Press 2009.
8. Jovitha Jerome, "Virtual Instrumentation using Lab view" PHI, 2010.
9. Woon- Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture', John Wiley & Sons, Inc., Hoboken, New Jersey 2007
10. Dogan Ibrahim, 'Advanced PIC microcontroller projects in C', Elsevier 2008

Skill Assessment:

1. Do a project: Home automation using Raspberry Pi Microcontroller
2. Write a detailed report on comparison between Arduino and Raspberry Pi Microcontroller.

Course Code:	24ES252	Course Title:	EMBEDDED PROGRAMMING LABORATORY
Credits:	2	L – T – P	0-0-4

Course objectives:

- To practice on Freeware soft wares/ Platforms.
- To develop an algorithm & programming on Software & Modelling tools and PLC/SCADA/PCB
- To expertise in GUI Simulators and Linux programming.
- To do hands-on in Programming & Simulation in Python Simulators.
- To practicing through Programming with wired/wireless Communication Protocols.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Interactive Simulations
2. Lab experiment videos
3. Blended Mode of Learning
4. Project based Learning
5. Experiential Learning
6. NPTEL and Other Videos
7. Smart Class Room
8. Flipped Class

DOMAIN	EXPERIMENT DETAILS	EQUIPMENT/ SUPPORTS REQUIRED
1.	Programming in Freeware soft wares/ Platforms	Programming Compilers & Platforms on freeware
2.	Software & Modelling tools Study on MEMS Tools Study on process Controller modelling PLC/SCADA/PCB one type CAD Tool	Personal Computers, Software & programming/modelling tools
3.	Programming & Simulation in GUI Simulators /Tools/others Graphical User interface simulations &modelling of instrumentation & controllers	Simulation Tools as LabVIEW /others
4.	Programming & Simulation in Python Simulators/Tools/others.	Programming in Python Platform

5.	Programming with wired/wireless Communication Protocols / Network Simulators	Learning Communication Protocols & Support Software Tools for BUS & network communication
6.	Linux programming Tool chain	PC with Linux OS

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Optimize the code for Freeware soft wares/ Platforms.
CO2	Develop solution for Software & Modelling tools and PLC/SCADA/PCB.
CO3	Develop a model using GUI Simulators for instrumentation & controllers and Graphical User interface.
CO4	Propose a solution for wired/wireless Communication Protocols using Network Simulators.
CO5	Develop programming concepts to knowledge upgradation on Python Simulators.

COs and POs Mapping:

CO/PO	PO1	PO2	PO3
CO1	3	-	2
CO2	3	-	2
CO3	3	-	2
CO4	3	-	2
CO5	3	-	2
CO	3	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of Assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	Model Exam	100	60	60	60
End Semester Examination (ESE)	Practical Exam	100	40	40	40
Total					100

Course Code:	24ES301	Course Title:	Software For Embedded Systems
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To expose the students to the fundamentals of embedded Programming.
- To Introduce the GNU C Programming Tool Chain in Linux.
- To study the basic concepts of embedded C.
- To teach the basics of Python Programming
- To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. PowerPoint presentation
3. Interactive Simulations
4. Lab experiment videos
5. Blended Mode of Learning
6. Project based Learning
7. Experiential Learning
8. NPTEL and Other Videos
9. Smart Class Room
10. Flipped Class

UNIT I - Basic C Programming**[9 hours]**

Typical C Program Development Environment - Introduction to C Programming - Structured Program Development in C - Data Types and Operators - C Program Control - C Functions - Introduction to Arrays.

UNIT II – Embedded C**[9 hours]**

Adding Structure to 'C' Code: Object oriented programming with C, Header files for Project and Port, Examples. Meeting Real-time constraints: Creating hardware delays - Need for timeout mechanism - Creating loop timeouts - Creating hardware timeouts.

UNIT III – C Programming Tool-Chain In Linux	[9 hours]
C preprocessor - Stages of Compilation - Introduction to GCC - Debugging with GDB - The Make utility - GNU Configure and Build System - GNU Binary utilities - Profiling - using gprof - Introduction to GNU C Library.	

UNIT IV – Python Programming	[9 hours]
Introduction - Parts of Python Programming Language - Control Flow Statements - Functions - Strings - Lists - Dictionaries - Tuples and Sets.	

UNIT V –Modules, Packages And Libraries In Python	[9 hours]
Python Modules and Packages - Creating Modules and Packages - Practical Example - Libraries for Python - Library for Mathematical functionalities and Tools - Numerical Plotting Library - GUI Libraries for Python - Imaging Libraries for Python - Networking Libraries.	

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Demonstrate C programming and its salient features for embedded systems
CO2	Deliver insight into various programming languages/software compatible to embedded process development with improved design & programming skills.
CO3	Develop knowledge on C programming in Linux environment.
CO4	Possess ability to write python programming for Embedded applications.
CO5	Have improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded programming skills.

COs and POs Mapping:

COs	PO1	PO2	PO3
CO1	-	-	2
CO2	1	-	1
CO3	-	2	-
CO4	1	-	1
CO5	-	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	25
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
Continuous Internal Examination (CIE) - Laboratory	Continuous Assessment	75	75	100	25
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Theory Exam	100	35	50	50
	Lab Exam	100	15		
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. A Cyber-Physical Systems Approach,. Second Edition, MIT Press, 2017.

Reference Books:

1. Fabrizio Romano, “Learn Python Programming”, Second Edition, Packt Publishing, 2018.

Web Links and Video Lectures (E-Resources):

Embedded Systems Design: https://onlinecourses.nptel.ac.in/noc20_cs14/preview

PROFESSIONAL ELECTIVE – I

Course Code:	24ES205	Course Title:	Wireless And Mobile Communication
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To study the Channel planning for Wireless Systems
- To study the Mobile Radio Propagation and Equalization and Diversity
- To study the Equalization and Diversity
- To provide insight about wideband code division based access.
- To study the Wireless multiple access and IP

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. NPTEL and Other Videos
3. Smart Classroom
4. Flipped Class

UNIT I –I The Cellular Concept	[9 hours]
System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies-Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity –Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems-Cell Splitting, Sectoring.	

UNIT II – Mobile Radio Propagation: Large-Scale Path Loss	[9 hours]
Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, Diffraction-Fresnel Zone Geometry, Knife edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models-Longley-Ryce Model, Okumura Model, Hata Model, Indoor Propagation Models-Partition losses, Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modelling.	

UNIT III – Mobile Radio Propagation	[9 hours]
Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel-Relationship between Bandwidth and Received power, Small-Scale Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time	

Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Nonlinear Equalization

UNIT IV – Wideband Code Division Multiple Access

[9
hours]

CDMA system overview -air interface –physical and logical channel–speech coding, multiplexing and channel coding –spreading and modulation: frame structure, spreading codes-uplink-downlink – 3G physical layer procedures: cell search and synchronization-establishing a connection-power controlhandover-overload control.

UNIT V – IP Mobility Framework

[9
hours]

Challenges of IP Mobility -Address Management -Dynamic Host Configuration Protocol and Domain Name Server Interfaces –Security –Mobility-Based AAA Protocol -IP Mobility Architecture Framework -x Access Network -IPv6 Challenges for IP Mobility.

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Understand Cellular communication concepts
CO2	Explain the mobile radio propagation
CO3	Perceive the wireless network different type of MAC protocols
CO4	Analyse the Equalization and Diversity
CO5	Build the Wireless multiple access and IP

COs and POs Mapping:

CO'S	PO1	PO2	PO3
CO1	3	3	2
CO2	3	3	2
CO3	3	3	2
CO4	1	-	-
CO5	1	-	-
CO	3	3	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal	CIE – I	100	50	10	40

Examination (CIE) - Theory	CIE – II	100		0	
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 13 marks question (either or).
- One 16 marks question (either or) will be from any one of the five units.
- All the sixteen questions have to be answered.

REFERENCE BOOKS

1. Wireless Communications, Principles, Practice –Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications Andrea Goldsmith, 2005 Cambridge University Press.
3. Principles of Wireless Networks –KavehPahLaven and P. Krishna Murthy, 2002, PE
4. Mobile Cellular Communication –GottapuSasibhushana Rao, Pearson Education, 2012.
5. Wireless Digital Communications –KamiloFeher, 1999, PHI.
6. Wireless Communication and Networking –William Stallings, 2003,

Course Code:	24ES206	Course Title:	VIRTUAL INSTRUMENTATION
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- Difference between Conventional and graphical programming.
- Basics of Lab VIEW and programming concepts.
- Real time and virtual instrument.
- Signals acquire process in digital domain.
- Concepts of data acquisition with LabVIEW.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Interactive Simulations
3. Lab experiment videos
4. Blended Mode of Learning
5. Project based Learning
6. Experiential Learning
7. NPTEL and Other Videos
8. Smart Classroom
9. Flipped Class

UNIT I – I FUNDAMENTALS OF VIRTUAL INSTRUMENTATION**[9
hours]**

Fundamental Concepts of Virtual Instrumentation (VI) and Graphical Programming - Virtual instruments and Traditional instruments, Hardware and Software in virtual instrumentation, Data Flow Programming - Data Types – Customization of VI Properties - VI Documentation.

UNIT II – PROGRAMMING STRUCTURES**[9
hours]**

Software Environment - Modular programming - Formula Nodes - Loops - Shift Registers - Local and Global Variables – Case and Sequence Structures - Arrays and Clusters - Graphs and Charts – State Machines - String and File I/O.

UNIT III – DATA ACQUISITION AND INTERFACING STANDARDS**[10
hours
]**

PC based data acquisition – DAQ hardware and software architecture – DAQ hardware configuration, sampling methods and grounding techniques, analog I/O, digital I/O, counter/timer - Communication: Interfacing of external instruments to a PC - RS232 - RS485 - GPIB – System Interface Buses: USBPCI, PXI; Introduction to bus protocols of MOD bus and CAN bus - Industrial Ethernet.

UNIT IV – ADVANCED PROGRAMMING**[10
hours
]**

Introduction, Definition of State Machine, A Simple State Machine, Event Structures. File Input / Output: Introduction, File Formats, File I/O Functions, Path Functions, Sample VIs to Demonstrate File WRITE and READ Function String Handling: Introduction, String Functions,

Lab VIEW String Formats, Typical examples Use of analysis tools and application of VI: Fourier transforms, Power spectrum, Simulation of systems using VI: Development of Control system, Image acquisition and processing.

UNIT V – CASE STUDIES

[7
hours
]

Temperature Monitoring System using PC based Data Acquisition System - Machine vision, Motion control, Configuration of Real-Time I/O Hardware in MAX - Host & Target VI – Prioritization of Tasks – Timed Programming Structures in Lab VIEW – Real-Time Application Deployment using my RIO – Run-time Interaction with Deployed Applications – Running Web Services in my RIO.

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Infer and interpret the fundamentals of Virtual Instrumentation and data Acquisition.
CO2	Explain the difference between the traditional and virtual instrumentation.
CO3	Illustrate the theoretical concepts to realize practical systems.
CO4	Analyze and evaluate the performance of Virtual Instrumentation Systems
CO5	Build a VI system to solve real time problems using data acquisition

COs and POs Mapping:

COs	PO1	PO2	PO3
CO1	-	2	1
CO2	-	-	2
CO3	1	3	3
CO4	2	2	3
CO5	3	3	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of Assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		

	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

TEXTBOOKS

1. Gary Johnson and Richard Jennings, —Lab VIEW Graphical Programming, McGraw Hill Inc., Fourth Edition, 2006
2. Lisa K Wells, “Lab view for Everyone”, Graphical programming made even easier, Prentice Hall of India.
3. LabVIEW programming, data acquisition and analysis, Beyon Jeffery Y, National instrument Virtual instrument series

REFERENCE BOOKS

1. Jovitha Jerome, —Virtual Instrumentation using Lab VIEW", PHI Learning Pvt. Ltd., 2010.
2. Sanjay Gupta and Joseph John, "Virtual Instrumentation Using Lab VIEW", Tata McGraw Hill, 2008.
3. Rick Bitter, Taqi Mohiuddin and Matt Nawrocki, "Lab VIEW Advanced Programming Techniques", CRC Press, 2009.
4. Clyde F Coombs, —Electronic Instruments Handbook, McGraw Hill Inc., Third Edition, 1999.

WEB LINKS AND VIDEO LECTURES (E-RESOURCES):

1. Virtual Instrumentation and Sensors: https://youtu.be/zlfCJ_wZA4Q?si=oNXQ-fSmQnTi6_dq
2. Data Acquisition systems: https://youtu.be/I_9Pwyxhe40?si=AMiwDjvq2A0-6Ioe
3. Interfacing Standards and design process: <https://youtu.be/T5jWYrnUWTc?si=vBbm3wOmpUbAlcjM>
4. LabVIEW Programming: <https://youtu.be/mBSB9qCf154?si=sGjEZRO4vNsi--c->

Course Code:	24ES207	Course Title:	Embedded Processor Development
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To learn about basic concepts of embedded system
- To learn about ARM architecture
- To learn C language and assembly programming.
- To learn Object orientation for programming and C++.
- To learn software modelling fundamentals.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Embedded Concepts**[9
hours]**

Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools

UNIT II – Arm Architecture and Overview of Cortex**[9
hours]**

Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture. Overview of Cortex-M3. Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions. Cortex-M3 Implementation Overview: Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.

UNIT III – CORTEX-M3/M4 Programming**[9
hours]**

Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software

Interface

Standard), Using Assembly Exception Programming: Using Interrupts, Exception/Interrupt Handlers,

Software Interrupts, Vector Table Relocation. Memory Protection Unit and other Cortex-M3 features:

MPU Registers, Setting Up the MPU, Power Management, Multiprocessor Communication

UNIT IV – Unified Modeling Language

[9
hours]

Connecting the object model with the use case model – Key strategies for object identification – UML

basics. Object state behaviour – UML state charts – Role of scenarios in the definition of behaviour –

Timing diagrams – Sequence diagrams – Event hierarchies – types and strategies of operations – Architectural design in UML concurrency design – threads in UML.

UNIT V – Embedded Software Development Tools and RTOS

[9
hours]

The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Demonstrate about basic concepts of embedded system
CO2	Build ARM architecture
CO3	Understand C language and assembly programming.
CO4	Build and compile Object orientation for programming and C++.
CO5	Create software modelling

COs and POs Mapping:

CO'S	1	2	3
CO1	2	3	1
CO2	3	-	3
CO3	-	-	2
CO4	-	-	3

CO5	2	-	3
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Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, econd Edition, Elsevier Inc. 2010.
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
3. David Seal “ARM Architecture Reference Manual”, 2001 Addison Wesley, England; Morgan Kaufmann Publishers
4. Andrew N Sloss, Dominic Symes, C0hris Wright, “ARM System Developer's Guide -Designing and Optimizing System Software”, 2006, Elsevier.
5. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education.
6. Cortex-M series-ARM Reference Manual .
7. Cortex-M3 Technical Reference Manual (TRM).
8. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual.
9. ARM Company Ltd. “ARM Architecture Reference Manual–RM DDI 0100E”.
10. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).
11. Ajay Deshmukh, “Microcontroller -Theory & Applications”, Tata McGraw Hill.
12. Arnold. S. Berger, “Embedded Systems Design -An introduction to Processes, Tools and Techniques”, Easwer Press.

13. David E. Simon, “An Embedded Software Primer”, Pearson Education, 2003.

Course Code:	24ES208	Course Title:	Automotive Embedded System
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To expose the students to the fundamentals and building of Electronic Engine Control systems.
- To teach on functional components and circuits for vehicles.
- To discuss on programmable controllers for vehicles management systems.
- To teach logics of automation & commercial techniques for vehicle communication.
- To introduce the embedded systems concepts for E-vehicle system development.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Basic of Electronic Engine Control Systems	[9 hours]
<p>Overview of Automotive systems, fuel economy, air-fuel ratio, emission limits and vehicle performance; Automotive microcontrollers- Electronic control Unit- Hardware & software selection and 37 requirements for Automotive applications – open source ECU- RTOS - Concept for Engine management-Standards; Introduction to AUTOSAR and Introduction to Society SAE- Functional safety ISO 26262- Simulation and modeling of automotive system components..</p>	

UNIT II – Sensors and Actuators for Automotives	[9 hours]
Review of sensors- sensors interface to the ECU, conventional sensors and actuators, Modern sensor and actuators - LIDAR sensor- smart sensors- MEMS/NEMS sensors and actuators for automotive applications.	

UNIT III – Vehicle Management Systems	[9 hours]
Electronic Engine Control-engine mapping, air/fuel ratio spark timing control strategy, fuel control, electronic ignition- Adaptive cruise control - speed control-anti-locking braking system- electronic suspension - electronic steering, Automatic wiper control- body control system; Vehicle system schematic for interfacing with EMS, ECU. Energy Management system for electric vehicles- Battery management system , power management system-electrically assisted power steering system Adaptive lighting system- Safety and Collision Avoidance.	

UNIT IV – Onboard Diagnostics and Telematics	[9 hours]
On board diagnosis of vehicles -System diagnostic standards and regulation requirements Vehicle communication protocols Bluetooth, CAN, LIN, FLEXRAY, MOST, KWP2000 and recent trends in vehicle communications- Navigation- Connected Cars technology – Tracking- Security for data communication- dashboard display and Virtual Instrumentation, multimedia electronics- Role of IOT in Automotive systems	

UNIT V – Electric Vehicles	[9 hours]
Electric vehicles –Components- Plug in Electrical vehicle- Charging station – Aggregators- Fuel cells/Solar powered vehicles- Autonomous vehicles.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Insight into the significance of the role of embedded system for automotive applications.
CO2	Illustrate the need, selection of sensors and actuators and interfacing with ECU
CO3	Develop the Embedded concepts for vehicle management and control systems.
CO4	Demonstrate the need of Electrical vehicle and able to apply the embedded system technology for various aspects of EVs
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systems design and its application in automotive systems.

COs and POs Mapping:

CO'S	1	2	3
CO1	-	2	1
CO2	2	3	2
CO3	3	3	3
CO4	3	3	3
CO5	3	3	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. D P Kothari and I.J Nagarath, “Basic Electrical and Electronics Engineering,” McGraw Hill Education (India) Private Limited, Second Edition, 2020
2. A.K.Sawhney and Puneet Sawhney, “A Course in Electrical & Electronic Measurements & Instrumentation,” Dhanpat Rai and Co, 2015.

Reference Books:

1. William B. Ribbens, “Understanding Automotive Electronics”, Elsevier, 2012
2. Ali Emedi, Mehrdedehsani, John M Miller, “Vehicular Electric power system- land, Sea, Air and Space Vehicles” Marcel Decker, 2004.

3. L.Vlacic,M.Parent,F.Harahima,"Intelligent VehicleTechnologies",SAE International,2001.
4. Jack Erjavec,JeffArias,"Alternate Fuel Technology-Electric ,Hybrid& Fuel Cell Vehicles",Cengage ,2012.
5. Electronic Engine Control technology – Ronald K Jurgen Chilton’s guide to Fuel Injection – Ford.
6. Automotive Electricals / Electronics System and Components, Tom Denton, 3 rd Edition, 2004.
7. Uwe Kiencke, Lars Nielsen, “Automotive Control Systems: For Engine, Driveline, and Vehicle”, Springer; 1 edition, March 30, 2000.
8. Automotive Electricals Electronics System and Components, Robert Bosch Gmbh, 4 th Edition, 2004.
9. Automotive Hand Book, Robert Bosch, Bently Publishers, 1997.
10. Jurgen, R., Automotive Electronics Hand Book.

PROFESSIONAL ELECTIVE - II

Course Code:	24ES212	Course Title:	Intelligent Control and Automation
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To Impart the knowledge of various optimization techniques and hybrid schemes.
- To introduce the concept, Analysis and implementation of ANN and Fuzzy logic controllers.
- To Emphasis the need for Genetic algorithm and its role for automation.
- To provide the basics of automation and its requirements
- To demonstrate the role of Intelligent controller in automation applications.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Artificial Neural Network & Fuzzy Logic	[9 hours]
ARTIFICIAL NEURAL NETWORK: Learning with ANNs, single-layer networks, multi-layer perceptrons, Back propagation algorithm (BPA) ANNs for identification, ANNs for control, Adaptive neuro controller. Fuzzy Logic Control: Introduction, fuzzy sets, fuzzy logic, fuzzy logic controller design, Fuzzy Modelling & identification, Adaptive Fuzzy Control Design.	
UNIT II – Genetic Algorithm	[9 hours]
Basic concept of Genetic algorithm and detail algorithmic steps- Hybrid genetic algorithm - Solution for typical control problems using genetic algorithm. Concept on some other search techniques like Tabu search, Ant-colony search and Particle Swarm Optimization.	
UNIT III – Hybrid Control Schemes	[9 hours]
Fuzzification and rule base using ANN–Neuro fuzzy systems-ANFIS–Optimization of membership function and rule base using Genetic Algorithm and Particle Swarm Optimization.	
UNIT IV – Automation	[9 hours]
Introduction to Automation - Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations- Industrial Automation -computer vision for automation- PLC and SCADA based Automation- IoT for automation- Industry 4.0.	
UNIT V – Intelligent Controller for Automation Application	[9 hours]
Applications of Intelligent controllers in Industrial Monitoring, optimization and control- Smart Appliances- Automation concept for Electrical vehicle- Intelligent controller and Automation for Power System.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Demonstrate the basic architectures of NN and Fuzzy logics
CO2	Design and implement GA algorithms and know their limitations.

CO3	Explain and evaluate hybrid control schemes and PSO
CO4	Interpret the significance of Automation concepts.
CO5	Develop the intelligent controller for automation applications.

COs and POs Mapping:

CO'S	1	2	3
CO1	1	1	1
CO2	2	2	3
CO3	3	2	2
CO4	3	2	2
CO5	3	-	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. Laurene V.Fausett, “Fundamentals of Neural Networks, Architecture, Algorithms, and Applications”, Pearson Education, 2008.
2. Timothy J.Ross, “Fuzzy Logic with Engineering Applications”, Wiley, Third Edition, 2010.

3. David E.Goldberg, “Genetic Algorithms in Search, Optimization, and MachineLearning”, Pearson Education, 2009.
4. W.T.Miller, R.S.Sutton and P.J.Webrose, “Neural Networks for Control”, MIT Press,1996.
5. Srinivas Medida, Pocket Guide on Industrial Automation for Engineers andTechnicians, IDC Technologies.
6. ChanchalDey and Sunit Kumar Sen, Industrial Automation Technologies, 1stEdition,CRC Press, 2022.

Course Code:	24ES213	Course Title:	Unmanned Aerial Vehicle
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To make the students to understand the basic concepts and components of UAV systems.
- To teach the UAV design concepts.
- To provide an insight about the hardware structure for UAVs.
- To emphasis the communication protocol requirements and control strategy for UAVs.
- To highlight the need and the role of UAVs for real time applications and development of realtime UAVs.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Introduction to UAV	[9 hours]
Overview and background - History of UAV –classification – societal impact and future outlook Unmanned Aerial System (UAS) components --models and prototypes – System Composition – applications.	

UNIT II – The Design of UAV Systems	[9 hours]
Introduction to Design and Selection of the System- Aerodynamics and Airframe Configurations- Characteristics of Aircraft Types- Design Standards-Regulatories and regulations - Design for Stealth-controlsurfaces-specifications.	

UNIT III – Hardwares for UAV s	[9 hours]
Real time Embedded processors for UAVs - sensors-servos-accelerometer –gyros-actuators- power supply- integration, installation, configuration, and testing –MEMS/NEMS sensors and actuators for UAVs- Autopilot – AGL.	

UNIT IV – Communication Payloads and Controls	[9 hours]
Payloads-Telemetry-tracking-Aerial photography-controls-PID feedback-radio control frequency range–modems-memory system-simulation-ground test-analysis-trouble shooting	

UNIT V – The Development of UAV Systems	[9 hours]
Waypoints navigation-ground control software- System Ground Testing- System In-flight Testing- Mini, Micro and Nano UAVs- Case study: Agriculture- Health- Surveying- Disaster Management and Defense.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Identify different hardware for UAV.
CO2	Determine preliminary design requirements for an unmanned aerial vehicle.
CO3	Design UAV system.
CO4	Identify and Integrate various systems of unmanned aerial vehicle.
CO5	Design micro aerial vehicle systems by considering practical limitations.

COs and POs Mapping:

COs	POs					
	1	2	3	4	5	6
CO1	1	3	2	-	-	2
CO2	3	3	3	-	-	2

C03	3	2	3	3	3	3
C04	-	-	2	3	3	2
C05	3	-	3	3	3	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. Reg Austin “Unmanned Aircraft Systems UAV design, development and deployment”, Wiley, 2010.
2. Paul G Fahlstrom, Thomas J Gleason, “Introduction to UAV Systems”, UAV Systems, Inc, 1998
3. Dr. Armand J. Chaput, “Design of Unmanned Air Vehicle Systems”, Lockheed Martin Aeronautics Company, 2001
4. Kimon P. Valavanis, “Advances in Unmanned Aerial Vehicles: State of the Art and the Road to Autonomy”, Springer, 2007
5. Robert C. Nelson, Flight Stability and Automatic Control, McGraw-Hill, Inc, 1998.

Course Code:	24ES214	Course Title:	DSP Based System Design
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- To understand various representation methods of DSP system
- To provide insight about different DSP algorithms
- To familiarize the various architectures of DSP system
- To perform analysis of DSP architectures and to learn the implementation of DSP system in programmable hardware
- To learn the details of DSP system interfacing with other peripherals

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Representation of DSP System

[9
hours]

Single Core and Multicore, Architectural requirement of DSPs - high throughput, low cost, low power, small code size, embedded applications. Representation of digital signal processing systems – blockdiagrams, signal flow graphs, data-flow graphs, dependence graphs. Techniques for enhancingcomputational throughput - parallelism and pipelining.

UNIT II – DSP Algorithms

[9
hours]

DSP algorithms - Convolution, Correlation, FIR/IIR filters, FFT, adaptive filters, sampling rateconverters, DCT, Decimator, Expander and Filter Banks. DSP applications. Computational characteristics of DSP algorithms and applications, Numerical representation of signals-word lengtheffect and its impact, Carry free adders, Multiplier.

UNIT III –System Architecture

[9
hours]

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture andMemory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. VLIW architecture. Basic performance issue in

pipelining, Simple implementation of MIPS, Instruction Level Parallelism, Dynamic Scheduling, Dynamic Hardware Prediction, Memory hierarchy. Study of Fixed point and floating point DSP architectures

UNIT IV – Architecture Analysis on Programmable Hardware

**[9
hours]**

Analysis of basic DSP Architectures on programmable hardware. Algorithms for FIR, IIR, Lattice filter structures, architectures for real and complex fast Fourier transforms, 1D/2D Convolutions, Winograd minimal filtering algorithm. FPGA: Architecture, different sub-systems, design flow for DSP system design, mapping of DSP algorithms onto FPGA.

UNIT V – System Interfacing

**[9
hours]**

Examples of digital signal processing algorithms suitable for parallel architectures such as GPUs and MultiGPUs. Interfacing: Introduction, Synchronous Serial Interface CODEC, A CODEC Interface Circuit, ADC interface.

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Evaluate the DSP system using various methods.
CO2	Design algorithm suitable for different DSP applications.
CO3	Explain various architectures of DSP system.
CO4	Implement DSP system in programmable hardware.
CO5	Build interfacing of DSP system with various peripherals.

COs and POs Mapping:

CO'S	1	2	3
CO1	-	3	-
CO2	3	3	3
CO3	-	3	-
CO4	3	-	3
CO5	2	-	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. Sen M Kuo, Woon Seng S Gan, Digital Signal Processors
2. Digital Signal Processing and Application with C6713 and C6416 DSK, RulphChassaing, Worcester Polytechnic Institute, A Wiley Interscience Publication
3. Architectures for Digital Signal Processing, Peter Pirsch John Weily, 2007
4. DSP Processor and Fundamentals: Architecture and Features. Phil Lapsley, JBier, AmitSohan, Edward A Lee; Wiley IEEE Press
5. K. K. Parhi - VLSI Digital Signal Processing Systems - Wiley – 1999.
6. RulphChassaing, Digital signal processing and applications with C6713 and C6416 DSK, Wiley, 2005
7. Keshab K Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, student Edition, Wiley, 1999.
8. Nasser Kehtarnavaz, Digital Signal Processing System Design: LabVIEW-Based Hybrid Programming, Academic Press, 2008

Course Code:	24ES215	Course Title:	Machine Learning and Deep Learning
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- Understanding about the learning problem and algorithms
- Providing insight about neural networks
- Introducing the machine learning fundamentals and significance
- Enabling the students to acquire knowledge about pattern recognition.
- Motivating the students to apply deep learning algorithms for solving real life problems.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Learning Problems and Algorithms**[9
hours]**

Various paradigms of learning problems, Supervised, Semi-supervised and Unsupervised algorithms

UNIT II – Neural Networks**[9
hours]**

Differences between Biological and Artificial Neural Networks - Typical Architecture, Common Activation Functions, Multi-layer neural network, Linear Separability, Hebb Net, Perceptron, Adaline, Standard Back propagation Training Algorithms for Pattern Association - Hebb rule and Delta rule, Hetero associative, Auto associative, Kohonen Self Organising Maps, Examples of Feature Maps, Learning Vector Quantization, Gradient descent, Boltzmann Machine Learning.

UNIT III – Machine Learning - Fundamentals & Feature Selections & Classifications**[9
hours]**

Classifying Samples: The confusion matrix, Accuracy, Precision, Recall, F1- Score, the curse of dimensionality, training, testing, validation, cross validation, overfitting, under-fitting the data, early stopping, regularization, bias and variance. Feature Selection, normalization, dimensionality reduction, Classifiers: KNN, SVM, Decision trees, Naïve Bayes, Binary classification, multi class classification, clustering.

UNIT IV –Deep Learning: Convolutional Neural Networks	[9 hours]
Feed forward networks, Activation functions, back propagation in CNN, optimizers, batchnormalization, convolution layers, pooling layers, fully connected layers, dropout, Examples of CNNs.	

UNIT V – Deep Learning: RNNS, Autoencoders and GANS	[9 hours]
State, Structure of RNN Cell, LSTM and GRU, Time distributed layers, Generating Text,Autoencoders: Convolutional Autoencoders, Denoising autoencoders, Variational autoencoders,GANs: The discriminator, generator, DCGANs	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Illustrate the categorization of machine learning algorithms.
CO2	Compare and contrast the types of neural network architectures, activation functions
CO3	Acquaint with the pattern association using neural networks
CO4	Elaborate various terminologies related with pattern recognition and architectures of convolutional neural networks
CO5	Construct different feature selection and classification techniques and advanced neural network architectures such as RNN, Autoencoders, and GANs

COs and POs Mapping:

CO'S	1	2	3
CO1	1	3	1
CO2	2	3	2
CO3	3	-	3
CO4	2	3	3
CO5	3	3	3

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final mark

					s
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. J. S. R. Jang, C. T. Sun, E. Mizutani, Neuro Fuzzy and Soft Computing - A Computational Approach to Learning and Machine Intelligence, 2012, PHI learning
2. Deep Learning, Ian Good fellow, Yoshua Bengio and Aaron Courville, MIT Press, ISBN: 9780262035613, 2016.
3. The Elements of Statistical Learning. Trevor Hastie, Robert Tibshirani and Jerome Friedman. Second Edition. 2009.
4. Pattern Recognition and Machine Learning. Christopher Bishop. Springer. 2006.
5. Understanding Machine Learning. Shai Shalev-Shwartz and Shai Ben-David. Cambridge University Press. 2017

AUDIT COURSES - I

Course Code:	24AC101	Course Title:	English for Research Paper Writing
Credits:	2	L – T – P	2-0-0

Course objectives:

To impart knowledge on the

- Teach how to improve writing skills and level of readability.
- Tell about what to write in each section.
- Summarize the skills needed when writing a Title.
- Infer the skills needed when writing the Conclusion.
- Ensure the quality of paper at very first-time submission

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Interactive Simulations
3. Blended Mode of Learning
4. Project based Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Introduction to Research Paper Writing**[6
hours]**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

UNIT II – Presentation Skills**[6
hours]**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III –Title Writing Skills**[6
hours]**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV – Result Writing Skills**[6
hours]**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V –Verification Skills	[6 hours]
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission.	

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Understand that how to improve your writing skills and level of readability
CO2	Learn about what to write in each section
CO3	Understand the skills needed when writing a Title
CO4	Understand the skills needed when writing the Conclusion
CO5	Ensure the good quality of paper at very first-time submission

COs and POs Mapping:

COs	PO1	PO2	PO3
CO1	2	2	2
CO2	2	3	2
CO3	1	2	1
CO4	2	3	2
CO5	2	3	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Theory Exam	100	65	60	60
Total					100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006

Reference Books:

1. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006

Web Links and Video Lectures (E-Resources):

1. English for Research Paper Writing: https://onlinecourses.swyam2.ac.in/ntr24_ed15/preview

Course Code:	24AC102	Course Title:	Disaster Management
Credits:	2	L – T – P	2-0-0

Course objectives:

To impart knowledge on the

- Summarize basics of disaster.
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Interactive Simulations
3. Blended Mode of Learning
4. Project based Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – Introduction	[6 hours]
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.	
UNIT II – Repercussions of Disasters and Hazards	[6 hours]
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	
UNIT III –Disaster Prone Areas in India	[6 hours]
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics	
UNIT IV – Disaster Preparedness and Management	[6 hours]
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.	
UNIT V –Risk Assessment	[6 hours]
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People’s Participation in Risk Assessment. Strategies for Survival	

Course outcomes: On completion of the course, the student will have the ability to:

CO1	Summarize basics of disaster
CO2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4	Describe the standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5	Develop the strengths of disaster management approaches

COs and POs Mapping:

COs	PO1	PO2	PO3
CO1	2	2	2
CO2	2	3	2
CO3	1	2	1
CO4	2	3	2
CO5	2	3	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
	Model Lab Exam	25	25		
End Semester Examination (ESE)	Theory Exam	100	65	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Text Books:

1. Goel S. L., Disaster Administration And Management Text And Case Studies”, Deep & Deep Publication Pvt. Ltd., New Delhi, 2009.
2. Nishitha Rai, Singh AK, “Disaster Management in India: Perspectives, issues and strategies “New Royal book Company, 2007.

Reference Books:

1. Sahni, Pardeep Et. Al. ,” Disaster Mitigation Experiences And Reflections”, Prentice Hall Of India, New Delhi, 2001.

Web Links and Video Lectures (E-Resources):

1. Disaster Management: https://onlinecourses.swayam2.ac.in/cec19_hs20/preview

Course Code:	24AC103	Course Title:	Constitution of India
Credits:	3	L – T – P	3-0-0

Course objectives:

To impart knowledge on the

- Understand the premises informing the twin themes of liberty and freedom from a civil right perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Blended Mode of Learning
3. Project based Learning
4. Experiential Learning
5. NPTEL and Other Videos
6. Smart Class Room
7. Flipped Class

UNIT I – History of Making of the Indian Constitution	[6 hours]
History, Drafting Committee, (Composition & Working) - Preamble, Salient Features	

UNIT II – Contours of Constitutional Rights and Duties	[6 hours]
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.	

UNIT III – Organs of Governance	[6 hours]
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.	

UNIT IV –Local Administration	[6 hours]
District’s Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat.Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Roleof Elected and Appointed officials, Importance of grass root democracy.	

UNIT V – Election Commission	[6 hours]
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
CO2	Discuss the intellectual origins of the framework
CO3	Discuss the intellectual origins of conceptualization of social reforms leading to revolution in India.
CO4	Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
CO5	Discuss the passage of the Hindu Code Bill of 1956.

COs and POs Mapping:

CO’S	1	2	3
CO1	-	1	-
CO2	-	1	-
CO3	-	1	-
CO4	-	1	-
CO5	-	1	-

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Reference Books:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr.S.N.Busi, Dr.B.R.Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.